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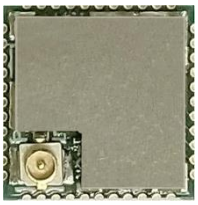
ITM-8510R

Multi-protocol Thread/Matter RF Module



Specification For ITM-8510R

V1.1

Revision History

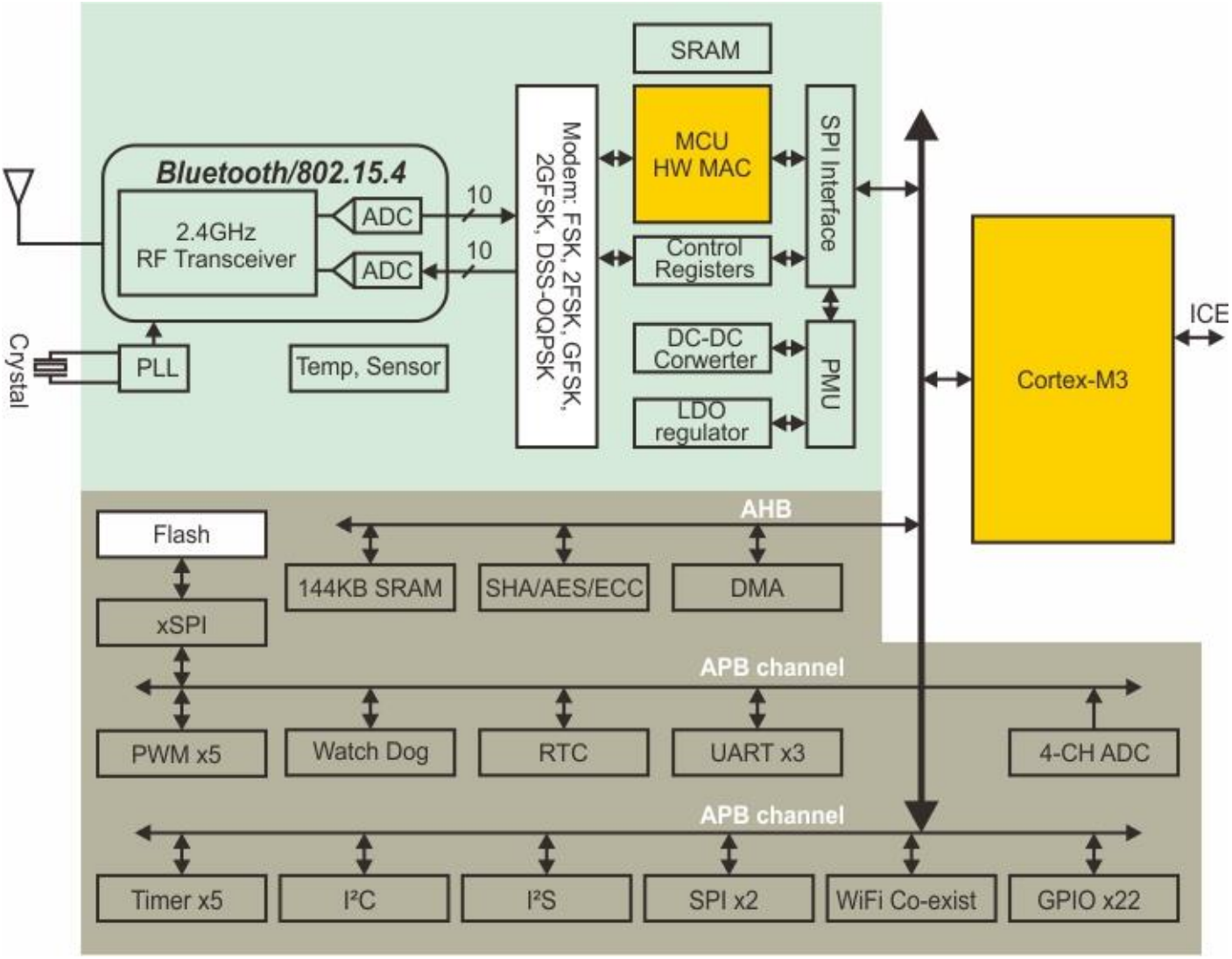
Date	Revision Content	Revised By	Version
2023/12/5	- Initial released	Ant Yang	1.1
	-		
	-		
	-		
	-		

Contents

1. General Description

The ITM-8510R is an ultra-low-power, high-performance ARM® Cortex®-M3-based Thread/Matter RF Module with multi-protocol Bluetooth Low Energy 5.3, Zigbee 3.0, Thread(IEEE®802.15.4)and proprietary 2.4G networking stacks to facilitate home & building automation, smart lighting, smart locks, sensor network applications, etc.A comprehensive mix of analog and digital peripherals are integrated with the 2.4GHz RF transceiver, which is compliant with Bluetooth Low Energy 5.3 and IEEE® 802.15.4 requirements. Ultra-low current consumption is achieved in the RF receive & transmit modes and power-down modes to support the latest IPv6-based IoT applications.

Block diagram of ITM-8510R Multiprotocol Thread/Matter RF Module:



Key Features:

- 2.4G RF transceiver supports below protocol stacks to meet IoT applications:
  - Bluetooth 5.x / BLE Mesh
  - IEEEE 802.15.4 (Zigbee 3.0 and Thread1.1)
  - 2.4GProprietary.
  - Multi-standards in Zigbee 3.0 + BLE 5.xconcurrently

Target Applications:

- Smart Home
- Smart Lighting ; Commercial / Industrial Mesh Lighting
- Building Automation
- Smart Energy Management
- IoT sensor network

2. Features

- Meets Bluetooth® 5.1 Low Energy and 802.15.4g Specifications, BQB Certified as a PHY component
- ARM Cortex-M3 (CM3) CPU64MHz
- 2MB Flash
- Embedded 208KB SRAM (144KB for CM3, 64KB for communication subsystem)
- Compliant with Bluetooth® 5.3 LE , ZigBee3.0
- High TX output power
  - **Bluetooth: +10dBm**
  - **Thread/Zigbee: +10dBm with <2% EVM**
- High RX sensitivity:
  - **Bluetooth: -104dBm @ 125Kbps,**
  - **Thread/Zigbee: -100dBm**
- Frequency Range: 2.402 ~2.480GHz
- Bluetooth Data Rates:125Kbps/500Kbps/1Mbps/2Mbps.
- Thread/Zigbee Data Rates:250Kbps
- Modulation: Multi-rate FSK, and OQPSK supported
- RSSI readout
- Integrated Security: SHA. AES,ECC
- HW crypto engine and security boot ; CRC,AES-CCM
- 10-bit ADC & DAC in 2.4GHzradio
- Peripherals
  - Watchdog
  - 1 x I^2Cinterface
  - 2 x SPI interface

- 3 x UART interface (1 with CTS/RTS, 2 with out CTS/RTS)
- 1 x I^2S
- 5 x PWM
- 3 x 32-bitTimer
- 2 x 32-bit RTC Timer
- 4-CH 10-bitADC
- 22 x GPIO
- DMA controller
- Internal 32KHzOscillator
- 32MHz Crystal and TCXO supported
- Integrated DC-DC converter and LDO regulator
- Power Saving Mode (Sleep and Deep Sleep Mode: (5.2/4.0/1.5μA)
- FW command mode: AT command mode and Transparent mode
- Operating Voltage: 1.8 ~3.6V
- Operating Temperature: -40 ~105°C
- ESD: HBM 2KV / MM 200V, Latch-up:150mA
- Halogen-free / RoHS 2.0 / Reach Annex 14 &17
- **Power consumption**

Power Consumption		TX(mA)	RX(mA)
BLE	PHY S8	25	15
	PHY S2	19	15
	1M	21	15
	2M	14	15
	4M	14	15
Zigbee		29	15

Power Consumption	Standby	5mA

3. Pin Assignments

<TOP View>

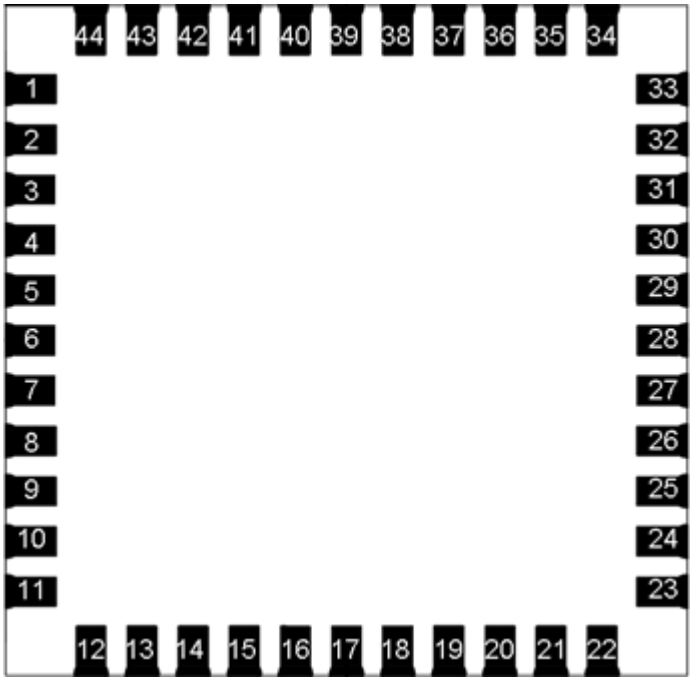


Table 1 Pin Assignments

ITM-8510R		
Pin NO.	Pin Name	Function
1	GND	Ground pin
2	RF_2.4G	2.4GHz RF input/output
3	GND	Ground pin
4	BUCK_IN	1.2VDC for LNA and RF blocks (2.4GHz)
5	NC	Floating (Don’t connected to ground)
6	NC	Floating (Don’t connected to ground)
7	GPIO31_UART2_RXD	multi-function digital I/O
8	GPIO30_UART2_TXD	multi-function digital I/O
9	VBAT	3.3VDC for Power Management Unit
10	GPIO29_UART1_RXD	multi-function digital I/O
11	GPIO28_UART1_TXD	multi-function digital I/O
12	POR_EXT	external Power-on Reset input
13	NC	Floating (Don’t connected to ground)
14	NC	Floating (Don’t connected to ground)
15	NC	Floating (Don’t connected to ground)

16	GPIO23	multi-function digital I/O
17	GPIO22	multi-function digital I/O
18	GPIO21	multi-function digital I/O
19	GPIO20	multi-function digital I/O
20	GND	Ground pin
21	NC	Floating (Don’t connected to ground)
22	VDD_IO	3.3VDC power for GPIO
23	GND	Ground pin
24	GPIO15	multi-function digital I/O
25	GPIO14	multi-function digital I/O
26	SWDIO	ARM MCU ICE data
27	SWCLK	ARM MCU ICE clock
28	GPIO9	multi-function digital I/O
29	GPIO8	multi-function digital I/O
30	GPIO7	multi-function digital I/O
31	GND	Ground pin
32	BUCK_OUT	DCDC feedback/output of internal 1.2V LDO
33	GND	Ground pin
34	GPIO6	multi-function digital I/O
35	GPIO5	multi-function digital I/O
36	GND	Ground pin
37	GPIO17_UART0_TXD	multi-function digital I/O
38	GPIO16_UART0_RXD	multi-function digital I/O
39	GPIO4	multi-function digital I/O
40	GPIO3	multi-function digital I/O
41	GPIO2	multi-function digital I/O
42	GPIO1	multi-function digital I/O
43	GPIO0	multi-function digital I/O
44	NC	Floating (Don’t connected to ground)

4. Physical Ratings

Table 2 Physical Ratings

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Storage temperature	T_{STG}	0	~	+ 45	ºC	
Operating temperature (ambient)	T_A	0	25	+ 45	ºC	

5. Electrical Ratings

Table 3 Electrical Ratings (Rx/Tx operating mode @ 25 ºC)

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
PMU input voltage	VDD_{3V}	1.8	3.3	3.6	V	
IO Operation Voltage	VDD_{IO}	1.8	3.3	3.6	V	

6. ESD Immunity

Table 4 ESD Immunity with VDD_{3V} = +3.3VDC @ 25 ºC

Characteristic	Symbol	Minimum	Unit	Condition
Machine Model	MM	± 200	V	
Human Body Model	HBM	± 2000	V	Class 2, ANSI/JEDEC JS-001
Human Body Model – RFIO pin	HBM	± 1000	V	Class 2, ANSI/JEDEC JS-001
Charged Device Model	CDM	± 500	V	Class C4, ANSI/ESD STM5.3.1
Latch-up Immunity	LU	150	mA	

Note: Stresses listed in Tables 3, 4 and 5 (above) may cause permanent damage to the device. These are stress ratings only. The functional operation is not implied at these or any other conditions, as well as those indicated in the operating listings of this specification. Exposure to maximum rating conditions for extended periods may affect device performance and/or reliability.

7. RF Performance Characteristics

Table 5 GFSK Transmitter Characteristics @ 2.4GHz with VDD_{3V} = +3.3VDC @ 25 ºC

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
RF Output Power	P_{OUT}	-10		+ 10	dBm	3.3VDC≦VDD_{3V}≦3.6VDC
Operating Frequency	$F_{OPERATING}$	2402		2480	MHz	
Frequency Drift	ΔF		< ± 50		kHz	1Mbps & 2Mbps data rates
Frequency Drift Rate	$F_{\Delta F}$		< ± 20		kHz /50µs	1Mbps & 2Mbps data rates
Average Frequency Deviation (data pattern = 111000…)	Δf1	225	250	275	kHz	1Mbps data rate
		450	500	550	kHz	2Mbps data rate
Instantaneous Deviation (data pattern = 10101010…)	Δf2	185			kHz	1Mbps data rate
		370			kHz	2Mbps data rate
Deviation Ratio	Δf2 / Δf1		80		%	1Mbps & 2Mbps data rates
Spectrum Mask with Adjacent Channel Offset: ± 2MHz			- 20		dBm	1Mbps data rate
Spectrum Mask with Adjacent Channel Offset: ≥ 3MHz			- 30		dBm	1Mbps data rate
Spectrum Mask with Adjacent Channel Offset: ± 4MHz			- 20		dBm	2Mbps data rate
Spectrum Mask with Adjacent Channel Offset: ± 5MHz			- 20		dBm	2Mbps data rate
Spectrum Mask with Adjacent Channel Offset: ± 6MHz			- 30		dBm	2Mbps data rate

Table 6 GFSK Receiver Characteristics @ 2.4GHz with VDD_{3V} = +3.3VDC @ 25 ºC

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
RF Sensitivity			- 93		dBm	2Mbps
			- 96		dBm	1Mbps
			- 99		dBm	500Kbps
			- 104		dBm	125Kbps
Carrier-to-Interference: Co-Channel Selectivity	C/I CO-CHANNEL		6.5		dBc	1Mbps
			6.5		dBc	2Mbps

Carrier-to-Interference: - 1MHz Adjacent Channel Selectivity	C/I - 1MHz		- 5		dBc	1Mbps
Carrier-to-Interference: + 1MHz Adjacent Channel Selectivity	C/I + 1 MHz		- 5		dBc	1Mbps
Carrier-to-Interference: - 2MHz Adjacent Channel Selectivity	C/I - 2MHz		- 25		dBc	1Mbps
			- 4		dBc	2Mbps
Carrier-to-Interference: + 2MHz Adjacent Channel Selectivity	C/I + 2MHz		- 35		dBc	1Mbps
			- 4		dBc	2Mbps
Carrier-to-Interference: - 3MHz Adjacent Channel Selectivity	C/I - 3MHz		- 35		dBc	1Mbps
Carrier-to-Interference: + 3MHz Adjacent Channel Selectivity	C/I + 3MHz		- 40		dBc	1Mbps
Carrier-to-Interference: - 4MHz Adjacent Channel Selectivity	C/I - 4MHz		- 24		dBc	2Mbps
Carrier-to-Interference: + 4MHz Adjacent Channel Selectivity	C/I + 4MHz		- 30		dBc	2Mbps
Carrier-to-Interference: - 6MHz Adjacent Channel Selectivity	C/I - 6MHz		- 35		dBc	2Mbps
Carrier-to-Interference: + 6MHz Adjacent Channel Selectivity	C/I + 6MHz		- 40		dBc	2Mbps
Carrier-to-Interference: Image Channel Selectivity	C/I IMAGE		- 25		dBc	1Mbps
			- 24		dBc	2Mbps
Carrier-to-Interference: Image -1MHz Adjacent Channel Selectivity	C/I IMAGE1MHz		- 35		dBc	1Mbps
Carrier-to-Interference: Image -2MHz Adjacent Channel Selectivity	C/I IMAGE2MHz		- 35		dBc	2Mbps
Intermodulation Interferer Level	IM		- 35		dBc	1Mbps
			- 25		dBc	2Mbps
Out-of-band Blocking: Interferer 30MHz ≤ f ≤ 2000MHz	OOB 30Mz, 2000MHz		- 15		dBm	1Mbps, 2Mbps
Out-of-band Blocking: Interferer 2003MHz ≤ f ≤ 2399MHz	OOB 2000MHz, 2399MHz		- 20		dBm	1Mbps, 2Mbps
Out-of-band Blocking: Interferer 2484MHz ≤ f ≤ 2997MHz	OOB 2484MHz, 2997MHz		- 20		dBm	1Mbps, 2Mbps
Out-of-band Blocking: Interferer 2997MHz ≤ f ≤ 6GHz	OOB 2997MHz, 6GHz		- 10		dBm	1Mbps, 2Mbps
Out-of-band Blocking: Interferer 6GHz ≤ f ≤ 12.75GHz	OOB 6GHz, 12.75GHz		- 10		dBm	1Mbps, 2Mbps

Note: Signal for C/I measurements = - 67dBm with modulated interference, BER = 0.1%

Table 7 DSSS-OQPSK Transmitter Characteristics @ 2.4GHz, 2MHz Bandwidth VDD_{3V} = +3.3VDC @ 25 ºC

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
RF Output Power		- 10		+ 10	dBm	
Operating Frequency		2405		2480	MHz	
EVM at rated TX power			2%			
Spectrum Mask with Adjacent Channel offset ±3.5MHz			- 20		dB	250Kbps

Table 8 DSSS-OQPSK Receiver Characteristics @ 2.4GHz, 2MHz Bandwidth VDD_{3V} = +3.3VDC @ 25 ºC

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
RF Sensitivity			- 100		dBm	
Carrier-to-Interference: Co-Channel Selectivity	$C/I_{CO-CHANNEL}$		1		dBc	
Carrier-to-Interference: - 5MHz Adjacent Channel Selectivity	C/I_{-5MHz}		- 25		dBc	
Carrier-to-Interference: + 5MHz Adjacent Channel Selectivity	C/I_{+5MHz}		- 30		dBc	
Carrier-to-Interference: - 10MHz Adjacent Channel Selectivity	C/I_{-10MHz}		- 45		dBc	
Carrier-to-Interference: + 10MHz Adjacent Channel Selectivity	C/I_{+10MHz}		- 45		dBc	
Carrier-to-Interference: Image Channel Selectivity	C/I_{IMAGE}		- 25		dBc	
Blocking other Channels: Interferer frequency < Desired frequency - 3 channel-spacing			- 50		dBc	
Blocking other Channels: Interferer frequency < Desired frequency - 3 channel-spacing			- 50		dBc	

Note: signal for C/I measurements = -82dBm with compliant OQPSK PHY interference, PER = 1%

8. Power

Table 9 Power Saving Modes

Mode	Internal Function Block								
	sLDO	LF OSC	XTAL	PLL	TX PA	RX	Cortex-M3 Platform	SRAM Retention	Communication Subsystem
Sleep 1	ON	ON	OFF	OFF	OFF	OFF	**sleep**	32KB	standby
Sleep 2	ON	ON	OFF	OFF	OFF	OFF	**sleep**	32KB	OFF
Deep sleep	ON	OFF	OFF	OFF	OFF	OFF	**OFF**	None	OFF

Table 10 Power Consumption (entire chip) with VDD_{3V} = +3.3VDC @ 25 ºC

* Receive & transmit current does not include the Cortex-M3 MCU domain current

Mode	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Sleep 1	I_{slp1}		5.2		uA	Low Power level sleep 1; wakeup by any event
Sleep 2	I_{slp2}		4.0		µA	Low Power level sleep 2; wakeup by any event
Deep sleep	I_{ds}		1.5		µA	Low Power level sleep 3; wakeup only by GPIO
Receive @ 1Mbps	$I_{RECEIVE}$		11.0		mA	Radio receiving @DCDC
Receive @ 2Mbps	$I_{RECEIVE}$		11.0		mA	Radio receiving @DCDC
Transmit @ 0dBm	I_{TX_0}		15.0		mA	Radio transmission @DCDC
Transmit @ +4dBm	I_{TX_+4}		17.0		mA	Radio transmission @DCDC
Transmit @ +10dBm	I_{TX_+10}		25.0		mA	Radio transmission @DCDC

9. Power Saving Modes

There are several power saving modes in the ITM-8510R that can be used to reduce the power consumption.

Wait-for-interrupt State

In this mode, only the clock to the Cortex-M3 is turned off while other clocks are kept running. Any enabled interrupt will resume the Cortex-M3 clock.

Sleep state

In sleep state, the 32MHz XTAL is powered off and only the LF OSC clock is active. All peripheral interfaces such as UART, SPI, I^2C, etc. are disabled. The RTC, the slow clock timer and GPIOs can be programmed to wake up the system. The data of some registers and memories are retained so the Cortex-M3 will continue running from where it stopped.

The communication subsystem can be optionally enabled to maintain active RF links. When enabled, to minimize power consumption in this condition the communication subsystem is only active during scheduled time windows. An interrupt from the communication subsystem can also wake-up the entire SoC.

Deep sleep state

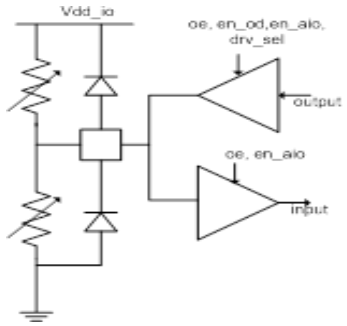
Deep sleep is the lowest power consumption mode with nearly the entire SoC powered off. Only GPIOs can be programmed to wake-up the system by defaults. If needed, LF OSC can be optionally enabled to wake-up the system. Waking from this power mode will re-boot the Cortex-M3.

10. Interfaces

IO

IO interfaces provide communication between the ITM-8510R and external ICs. They support several modes such as input mode,outputmode,opendrainmode,AnalogIOmodeandtheycanbeconfiguredbysoftware.TheIOinterfacescan also be configured by software to be SPI, UART, I^2C, I^2S, PWM and general purpose IO (GPIO). When used as GPIO, the input status also can be read by software and can be set to VDD_IO or GND bysoftware.

The basic IO architecture is:



The IO interfaces also provide several input pull modes and output driving modes.

Input pull modes:

- No pull(floating)
- Pull up to VDD_IO via 10K/100K/1M
- Pull down to GND via10K/100K/1M

Output driving currents:

- 4mA / 10mA / 14mA/ 20mA

Table 11 GPIO function mux for accessing peripherals

IO	SPI0	SPI1	UART	I^2C	PWM	I^2S
GPIO0(OD)	SPI0_CSN1/2/3					I2S0_BCK
GPIO1(OD)	SPI0_CSN1/2/3					I2S0_WCK
GPIO2(OD)	SPI0_CSN1/2/3					I2S0_SDO
GPIO3(OD)	SPI0_CSN1/2/3					I2S0_SDI
GPIO4(OD)	SPI0_SDATA2		UART1_TX			I2S0_MCLK
GPIO5(OD)	SPI0_SDATA3		UART1_RX			I2S0_MCLK
GPIO6(OD)	SPI0_SCLK		UART2_TX			
GPIO7(OD)	SPI0_CSN0		UART2_RX			
GPIO8(OD)	SPI0_SDATA0				PWM0	
GPIO9(OD)	SPI0_SDATA1				PWM1	
GPIO14(OD)	SPI0_SDATA2	SPI1_SDATA2	UART1_RTSN		PWM2	
GPIO15(OD)	SPI0_SDATA3	SPI1_SDATA3	UART1_CTSN		PWM3	
GPIO16(OD)			UART0_RX			
GPIO17(OD)			UART0_TX			
GPIO20(OD)			UART1_RTSN	SCL	PWM0/1/2/3/4	
GPIO21(OD)			UART1_CTSN	SDA	PWM0/1/2/3/4	
GPIO22(OD)				SCL	PWM0/1/2/3/4	
GPIO23(OD)				SDA	PWM0/1/2/3/4	
GPIO28(OD)(AIO4)	SPI0_SCLK	SPI1_SCLK	UART1_TX			
GPIO29(OD)(AIO5)	SPI0_CSN0	SPI1_CSN	UART1_RX			
GPIO30(OD)(AIO6)	SPI0_SDATA0	SPI1_SDATA0	UART2_TX			
GPIO31(OD)(AIO7)	SPI0_SDATA1	SPI1_SDATA1	UART2_RX			

- SDATA0 = MOSI, SDAT1 = MISO

SPI

The Serial Peripheral Interface either controls a serial data link as a master or reacts to a serial data link as a slave. Quad-bit mode (QSPI) is also supported.

The internal AHB bus controller can be configured by software to be a master or slave device. The maximum clock frequency is 16 MHz (Master mode) or 32 MHz (Slave mode). Core reading & writing is done on the AMBA AHB bus interface. The core operates in two data modes (8-bit or 32-bit). Data is serialized and then transmitted, either LSB or MSB first, using the standard 4-wire SPI bus interface or the extended Quad mode bus.

SPI interface features:

- 8- or 32-bit serial transmit &receive
- Half duplex operation
- Software programmable Master or Slave mode
- Quad-bit mode operation
- Dual-bit mode operation
- separate SCLK input for Master Mode
- 32-word Transmit FIFO
- 32-word Receive FIFO
- Interrupt control
- LSB or MSB mode
- Tristate Slave MISO signaling for multiple slaves
- DMA Interface
- Compatible with many industry-standard FLASH devices

UART

The ITM-8510R UART interface is compatible to 16450 and 16550.The three independent UARTs each have a maximum baud rate up to 2 Mbps.

UART interface features & supported baud rates:

- 16450 & 16550 Compatible Modes
- Programmablebaudratesupto2Mbps(2400/4800/9600/14400/19200/28800/38400/57600/76800/ 115200 / 500000 / 576000 / 1000000 / 2000000bps)
- FIFO and non-FIFO modes
- Transmit and Receive FIFOs
- Interrupt control
- Flow control

I²C

This is a standard I²C Master. A clock divider/clock select module customizes the frequency of the I²C portion of the module. Two separate FIFOs are used – one for storing up to 32 commands from the APB Interface, the other for storing up to 16 bytes of read data from the I²C Bus. The transmit engine reads commands from the command FIFO and executes these as I²C instructions. The receive engine monitors the I²C bus for slave responses and stores data in a Read Data FIFO, the contents of which are available to the processor on the APB Interface. Various conditions can cause an interrupt to be generated.

I²C interface features:

- Standard I²C (Inter-Integrated Circuit businterface)
- Master mode only
- Transmit and Receive Engine
- Clock Divider/ClockSelect
- Command FIFO and Read Data FIFO
- Interrupt Generation Logic
- Supports clock stretching
- Supports SCL arbitration

I²S

The I²S module transmits or receives audio samples with predefined protocols through GPIO. It supports two channels with I²S, LJ (Left Justified) and RJ (Right Justified) format. Two xDMA are also included in the I²S module to transfer audio samples between memory and the I²S module without CPU assistance.

I²S interface features:

- Master mode
- Master clock generator for MCLK
- Supports Tx, Rx and Tx+Rx
- Supports I²S, LJ and RJ format with16/32-BCK
- Supports 16/24/32-bit samplewidth
- Supports 8K, 16K, 32K and 48Kbps audio sample rates
- Supports DMA

PWM

The PWM module generates Pulse Width Modulated signals and drives the assigned GPIOs. It includes a pulse generator with up and up-and-down counting mode. Five PWM modules can provide up to 5 PWM channels and each channel can have its own individual frequency control for generation of the pulse width. A read-type xDMA is also in the PWM module to transfer frequency control between memory and the PWM module without CPU assistance.

PWM features:

- Programmable clock divider
- Five PWM modules and up to five channels for PWM
- PWM pulse generator with up and up-and-down counting mode
- Programmable duty-cycle sequence defined inmemory
- Duty-cycle sequence that can be repeated orloop-controlled

ADC

The ADC is an auxiliary differential successive-approximation analog-to-digital converter. The ADC module is used for measuring voltage from IO. Various sampling modes are provided and one DMA is included for the MCU to access memory written by the ADC.

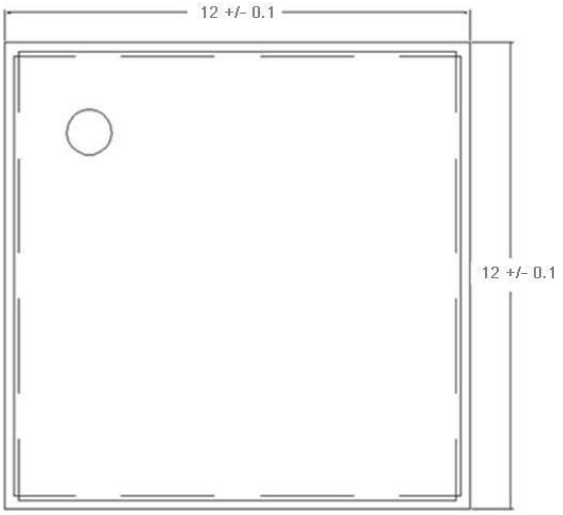
Features:

- 8/10/12-bit resolution and 14-bit resolution by oversampling
- One-shot, timer and scan mode for channel measuring
- One DMA to transfer ADC samples to memory with unsigned 16-bitformat
- Monitoring ADC sample results of eachchannel

11. Module Physical Dimensions

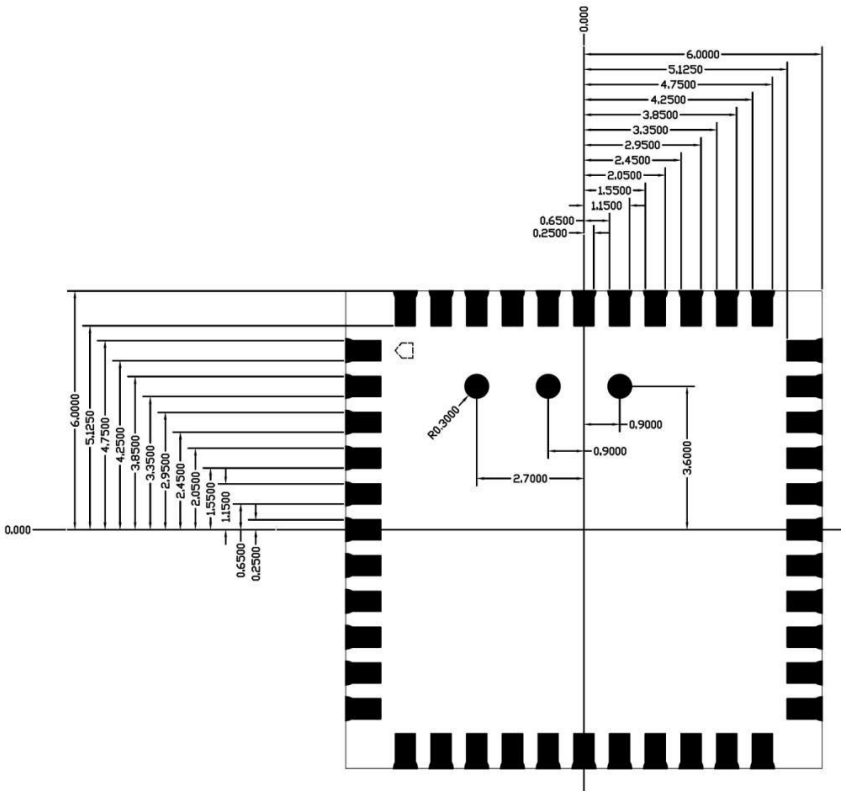
(UNIT:mm)

<TOP View>



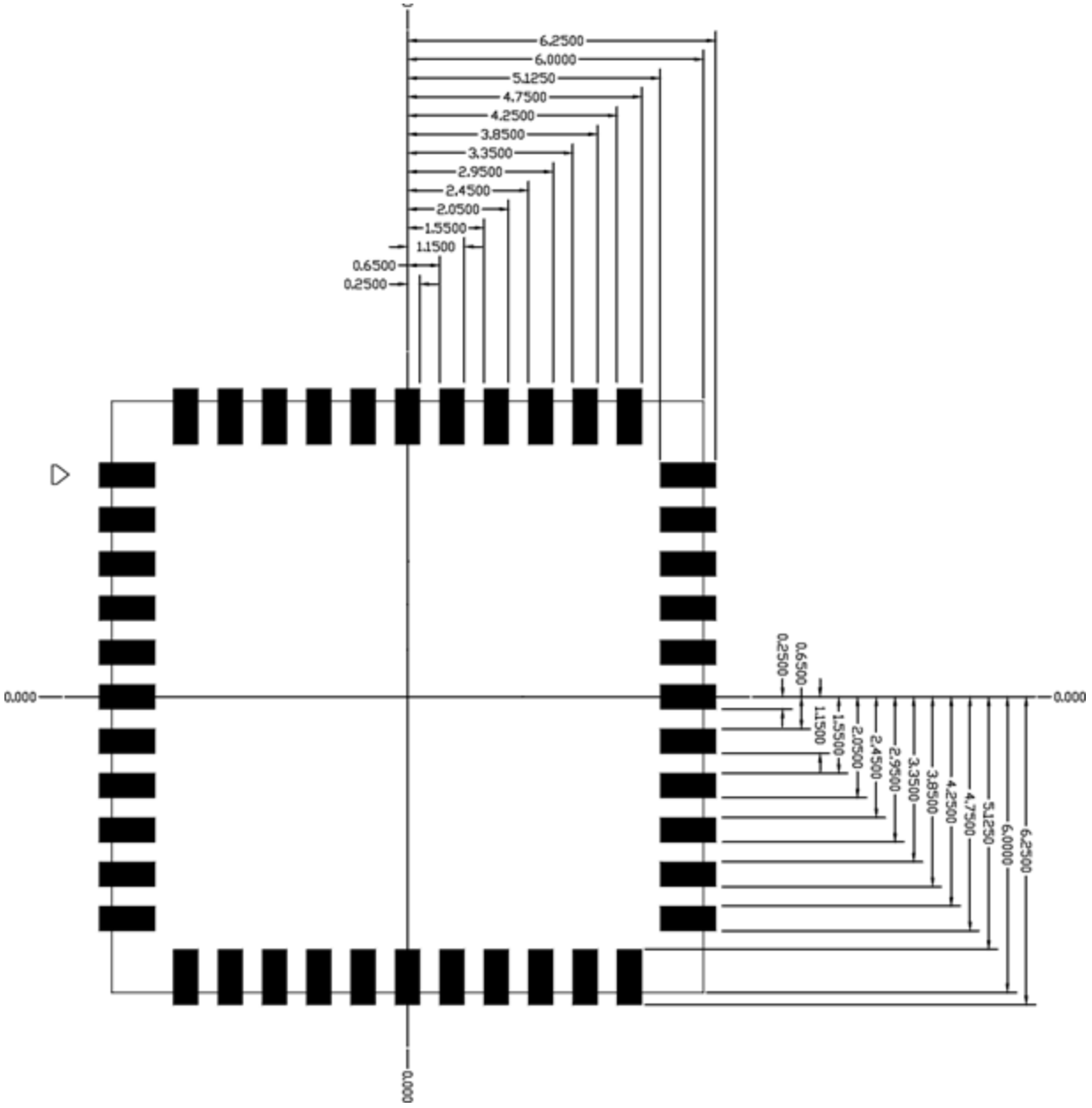
<SIDE View >

<TOP View>

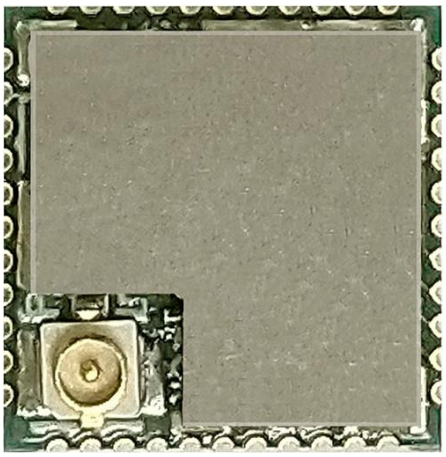


12. Module Layout Recommendation

(UNIT:mm)

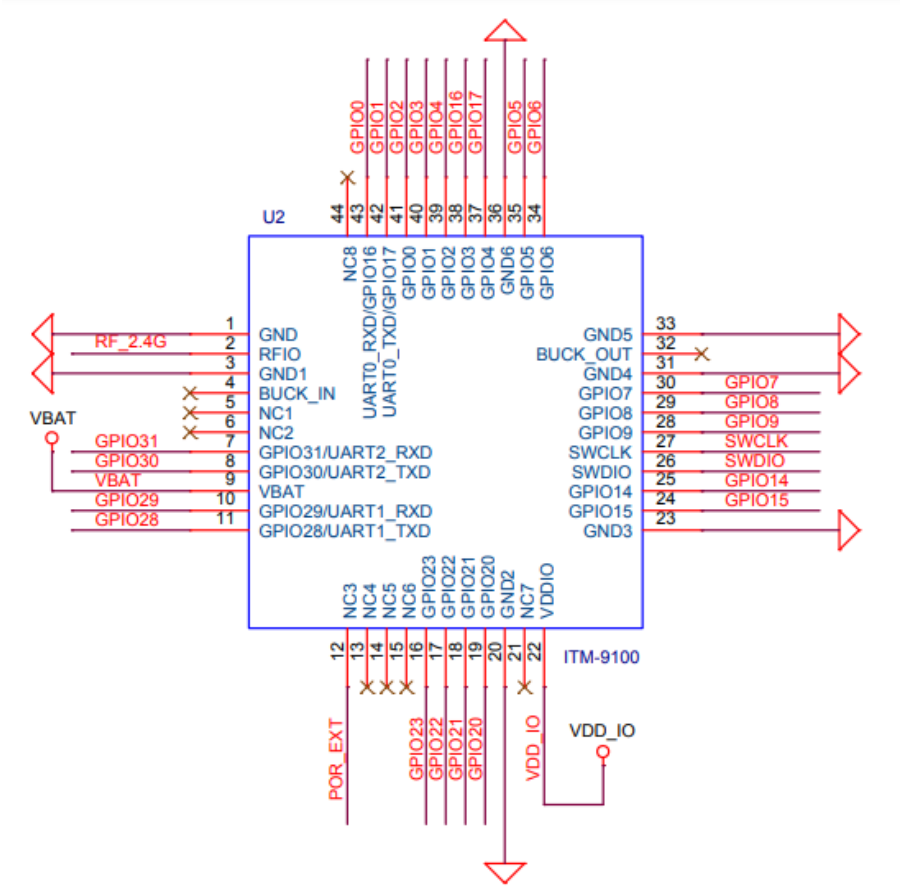


13. Module Outlook



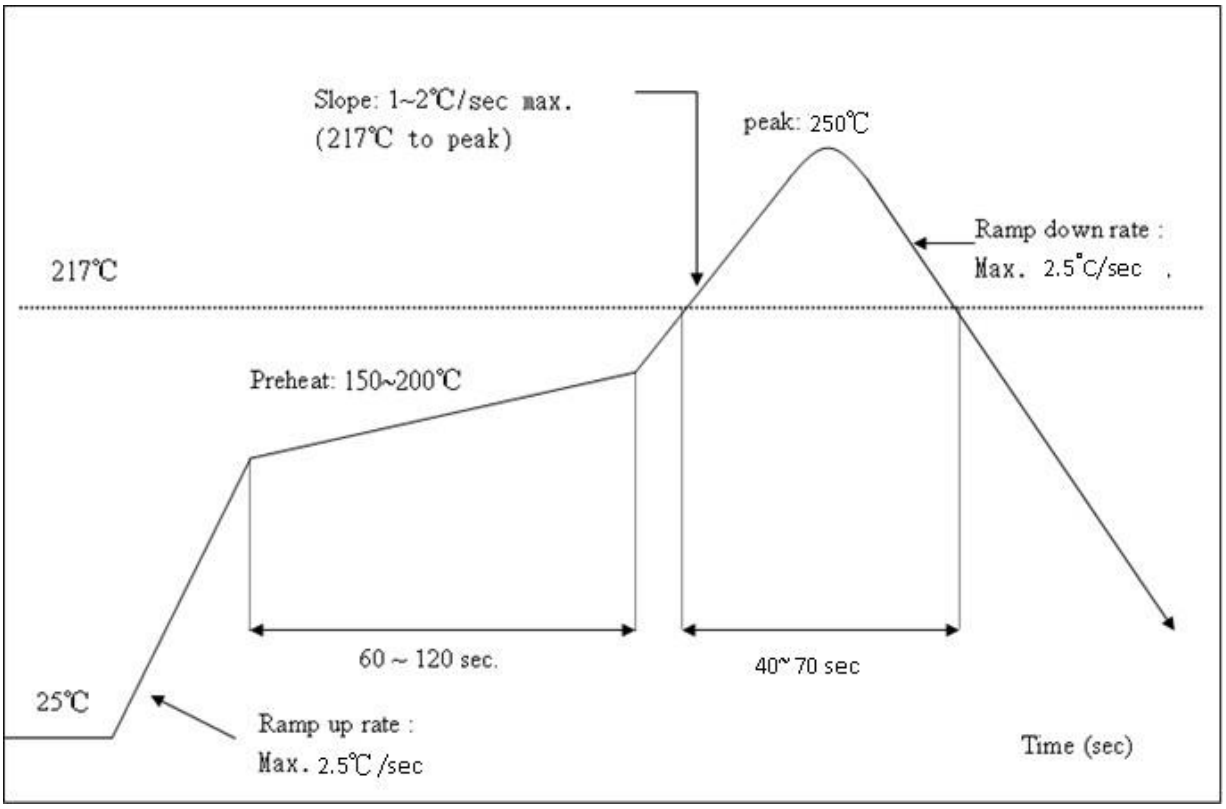
ITM-8510R

14. Reference Design



15. Recommended Reflow Profile

Referred to IPC/JEDEC standard. Peak
Temperature : <250°C Number of Times :
≤2 times

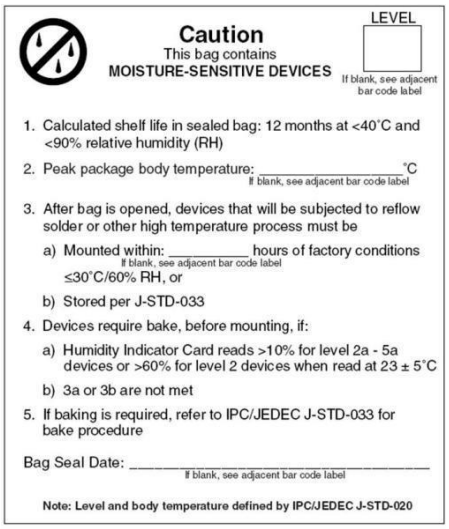


16. Packing Information

16.1 Label

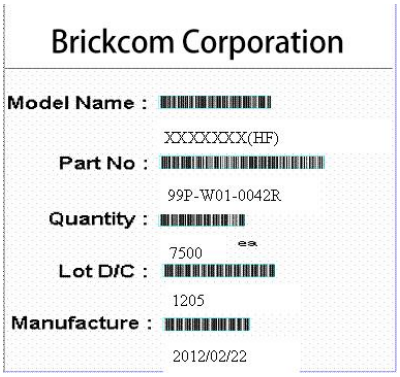
Label A →Anti-static and humidity notice

Label B →MSL caution / Storage Condition

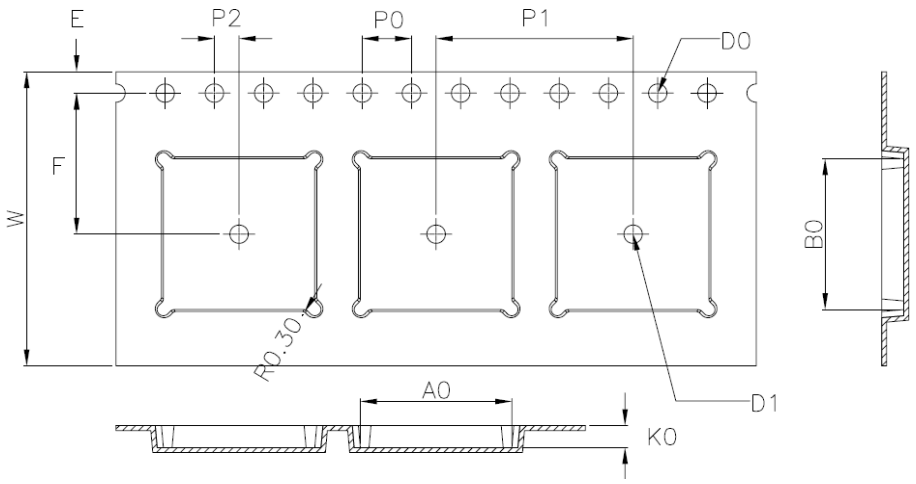


Label C →Inner box label .

Label D →Carton box label .

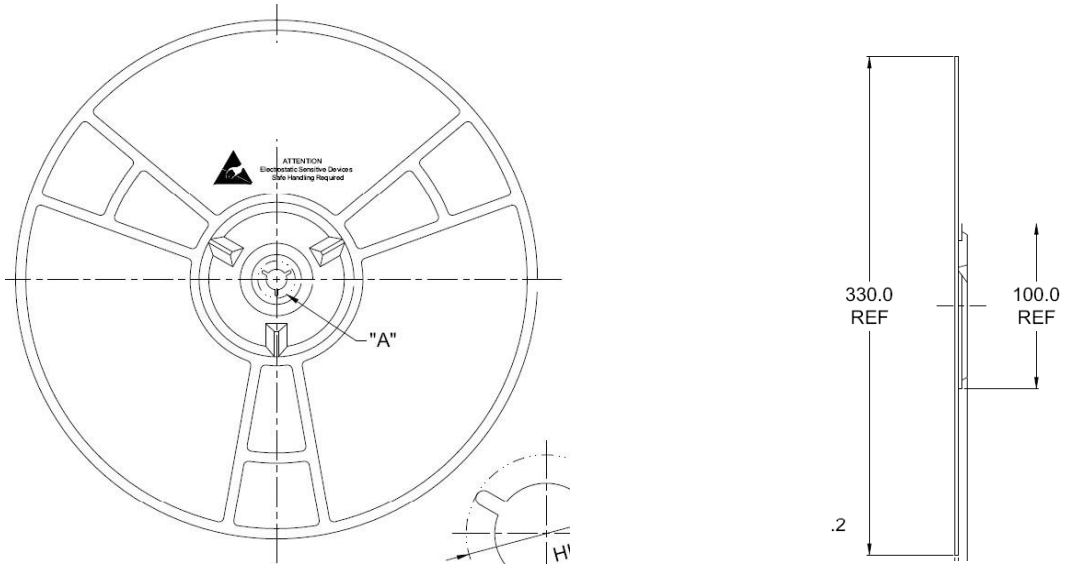


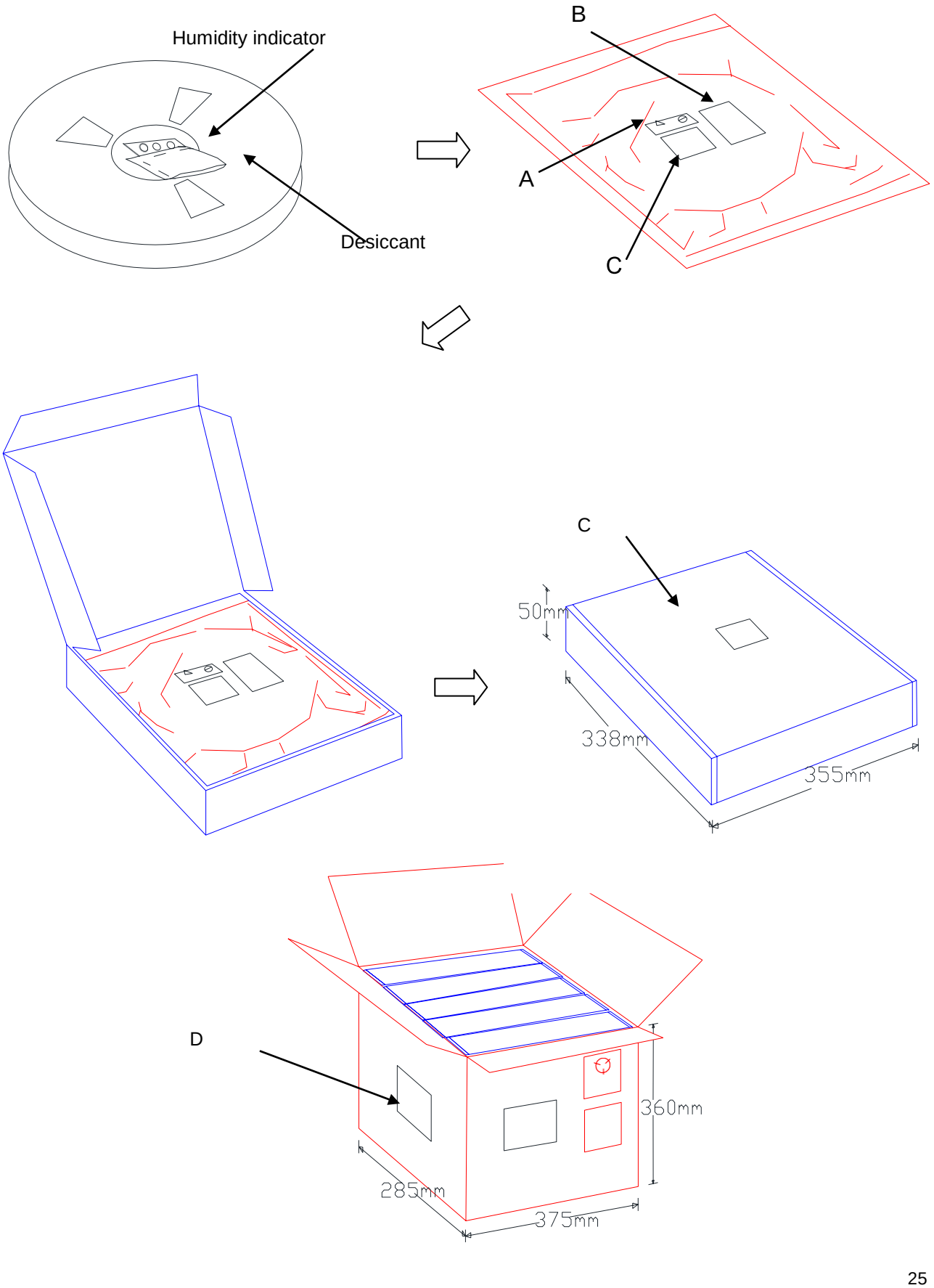
16.2 Dimension



W	24.00±0.30
A0	12.30±0.10
B0	12.30±0.10
K0	1.80±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	16.00±0.10
P2	2.00±0.10
D0	1.50 $^{+0.10}_{-0.00}$
D1	ø1.50MIN

1. 10 sprocket hole pitch cumulative toerance ±0.20
2. Carrier camber is within 1 mm in 250 mm
3. Material: Black Conductive Polystyrene Alloy
4. All dimensions meet EIA-481-D requirements
5. Thicjness: 0.30±0.05mm
6. Packing length per 22" reel: 98.5 Meters.(1:3)
7. Component load per 13" reel: 1500 pcs




Humidity indicator
Desiccant
B
A
C
C
50mm
338mm
355mm
D
360mm
285mm
375mm