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ITM-MV8-ANT / ITM-DV8

ITM-DV8

ITM-MV8-ANT

Datasheet

(Preliminary)

V0.3

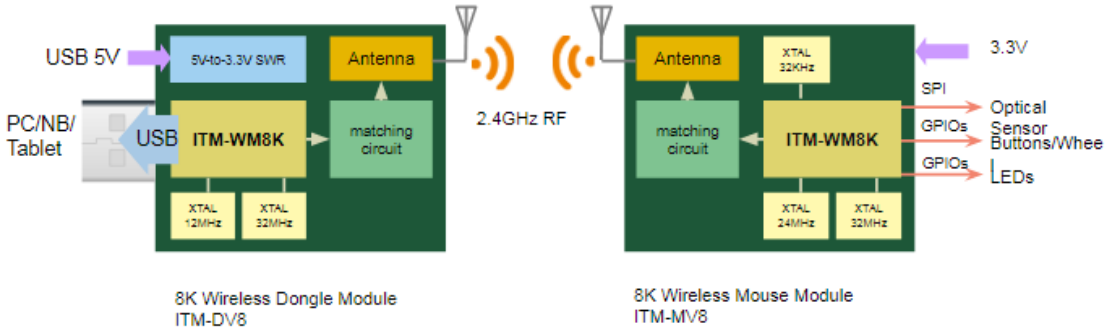
Revision History

Date	Revision Content	Revised By	Version
2022/07/06	- Initial released (Preliminary)	Marco Liu	0.1
2022/08/19	- Add Functional Description	HW	0.2
2022/12/28	- 1. Layout Recommendation - 2. Add wakeup Functional Description	HW	0.3
	-		
	-		

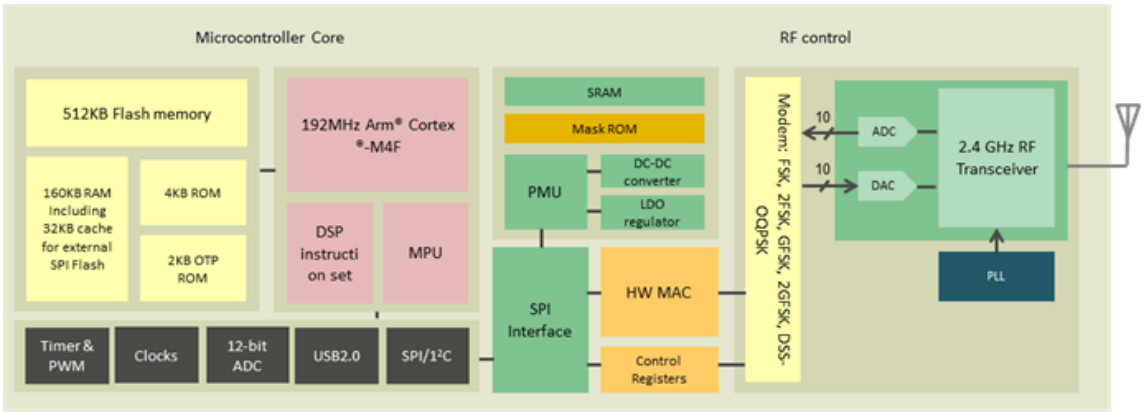
Contents

1. General Description

ITM-MV8-ANT and ITM-DV8 use Brickcom RF chipset ITM-WM8K to implement the world-wide first wireless mouse solution up to 8KHz polling rate. ITM-MV8-ANT is the module PCBA designed for the mouse side, connected to optical sensor, buttons, wheel, LEDs and 3.3V power source. ITM-DV8 is an USB dongle PCBA designed for the PC/NB side, to transmit/receive data to/from ITM-MV8-ANT. Via USB2.0 HS, ITM-DV8 can transfer mouse data from ITM-MV8-ANT to PC/NB with maximum 8KHz polling rate.



Block diagram of ITM-MV8-ANT / ITM-DV8



Block diagram of ITM-WM8K (USB2.0 feature is only available for ITM-DV8)

2. Features

2.1 ITM-MV8-ANT (Module for Mouse Side)

- Main Chipset: ITM-WM8K
  - MCU
    - ARM® Cortex®- M4F 32-bit processor , running up to 192 MHz
    - Built-in Memory Protection Unit (MPU)
    - Built-in Nested Vectored Interrupt Controller (NVIC)
    - Hardware IEEE 754 compliant Floating-point Unit (FPU)
    - DSP extension with hardware divider and single-cycle 32-bit hardware multiplier
    - 24-bit system tick timer / 32-bit Timer *4
    - Programmable and maskable interrupt
    - Low Power Sleep mode by WFI and WFE instructions
  - Memory
    - 512KB flash and 160KB (include 32 KB cache for XIP) RAM
    - 4KB ISP Loader ROM
  - Security
    - 96-bit Unique ID (UID)
    - 128-bit Unique Customer ID (UCID).
    - One built-in temperature sensor with 1°C resolution.
  - Wireless
    - 2.4GHz-2.5GHz proprietary RF transceiver
    - -20 to +10 dBm configurable TX power
    - -96 dB sensitivity at 1Mbps data rate
    - -93 dBm sensitivity at 2Mbps data rate
    - -87 dBm sensitivity at 4Mbps data rate
  - GPIOs
    - Total 28 GPIOs available
    - Support SPI/UART/I^2C/ADC function
- Antenna
  - Built-in chip antenna (Dimension L x W: 8.0X1.0mm)
  - External antenna can be connected when not using built-in antenna

2.2 ITM-DV8 (USB Dongle PCBA)

- Main Chipset : ITM-WM8K
  - MCU
    - ARM® Cortex®- M4F 32-bit processor , running up to 192 MHz
    - Built-in Memory Protection Unit (MPU)
    - Built-in Nested Vectored Interrupt Controller (NVIC)
    - Hardware IEEE 754 compliant Floating-point Unit (FPU)
    - DSP extension with hardware divider and single-cycle 32-bit hardware multiplier
    - 24-bit system tick timer / 32-bit Timer *4
    - Programmable and maskable interrupt
    - Low Power Sleep mode by WFI and WFE instructions
  - Memory
    - 512KB flash and 160KB (include 32 KB cache for XIP) RAM
    - 4KB ISP Loader ROM
  - Security
    - 96-bit Unique ID (UID)
    - 128-bit Unique Customer ID (UCID).
    - One built-in temperature sensor with 1°C resolution.
  - Wireless
    - 2.4GHz-2.5GHz proprietary RF transceiver
    - -20 to +10 dBm configurable TX power
    - -96 dBm sensitivity at 1Mbps data rate
    - -93 dBm sensitivity at 2Mbps data rate
    - -87 dBm sensitivity at 4Mbps data rate
  - USB
    - USB Specification reversion 2.0 compliant
    - Supports 12 configurable endpoints in addition to Control Endpoint
    - Supports DMA operation
    - 4092 Bytes Configurable RAM used as endpoint buffer
    - Supports Endpoint Maximum Packet Size up to 1024 bytes
- Antenna
  - Built-in chip antenna
- Power Supply
  - 4.5V~5.5V from USB bus power; Built-in 5V-to-3.3V switching LDO

3. General Specification

3.1 Voltages

3.1.1 Absolute Maximum Ratings

ITM-MV8-ANT

Symbol	Description	Min.	Max.	Unit
VDD	Input supply Voltage	-0.3	3.6	V

ITM-DV8

Symbol	Description	Min.	Max.	Unit
VDD	Input supply Voltage	-0.3	5.8	V

3.1.2 Recommended Operating Ratings

ITM-MV8-ANT

Test conditions: At operating temperature 0°C ~ 70°C				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VDD	3.0	3.3	3.6	V

ITM-DV8

Test conditions: At operating temperature 0°C ~ 70°C				
Symbol	**Min.**	**Typ.**	**Max.**	**Unit**
VDD	4.5	5.0	5.5	V

3.2 Wireless Specification (RX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2400		2500	MHz
RX Sensitivity < 30.8% PER	1Mbps		-96		dBm
	2Mbps		-93		dBm
	4Mbps		-87		dBm
Maximum Input Level			0		dBm

3.3 Wireless Specification (TX)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		2400		2500	MHz
Maximum Output Power		--	10	--	dBm
Power Control Range		-20		10	dB

3.4 Power Consumption

ITM-MV8-ANT

Active Mode @ 8KHz Report Rate 16.4 mA (Typical)

Low Power Mode:
- Deep LPS (Wakeup by GPIO/Timer) < 100uA (Typical)
- Power Down (Wakeup by RESET) < 50uA (Typical)

ITM-DV8

Active Mode @ 8KHz Report Rate 35.0mA (Typical)
Standby Mode 100uA (Typical)

4. Functional Description

4.1 Arm® Cortex® -M4F Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB- Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex®- M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®- M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The ITM-MV8 series is embedded with Cortex®-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. Figure 4.1-1 shows the functional controller of the processor.

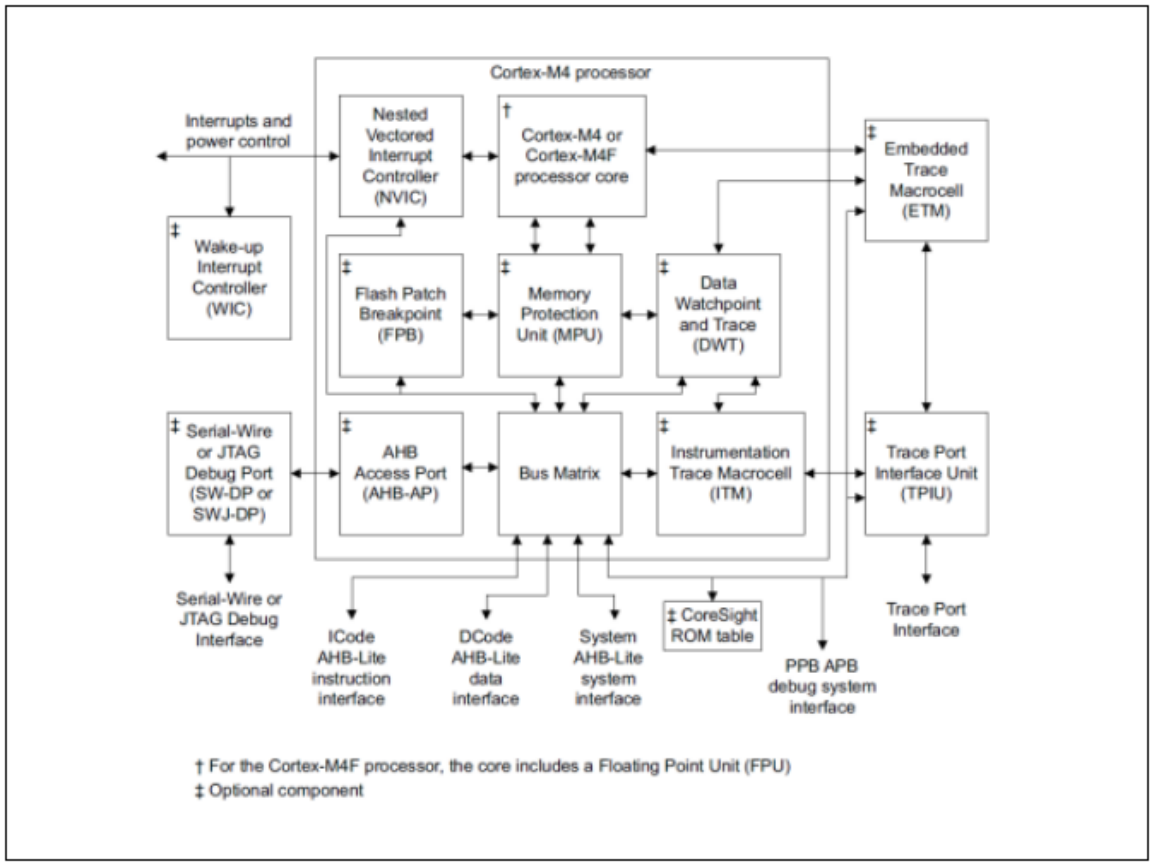


Figure 4.1-1 Cortex®-M4F Block Diagram

Cortex® -M4F processor features:

A low gate count processor core, with low latency interrupt processing that has:

- A subset of the Thumb instruction set, defined in the Armv7-M Architecture Reference Manual
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions, SDIV and UDIV
  - Handler and Thread modes
  - Thumb and Debug states
  - Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
  - Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
  - Support for Armv6 big-endian byte-invariant or little-endian accesses
  - Support for Armv6 unaligned accesses
- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the ITM-MV8 series configured with 64 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tril-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map

attributes

- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial Wire Debug Port(SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
  - Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and
  - code patches
  - Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
  - Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
  - Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
  - Optional Embedded Trace Macrocell (ETM) for instruction trace.
- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

4.2 System Manager

4.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

4.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source.

Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M4 core only by writing 1 to CPURST (SYS_IPRST0[1])

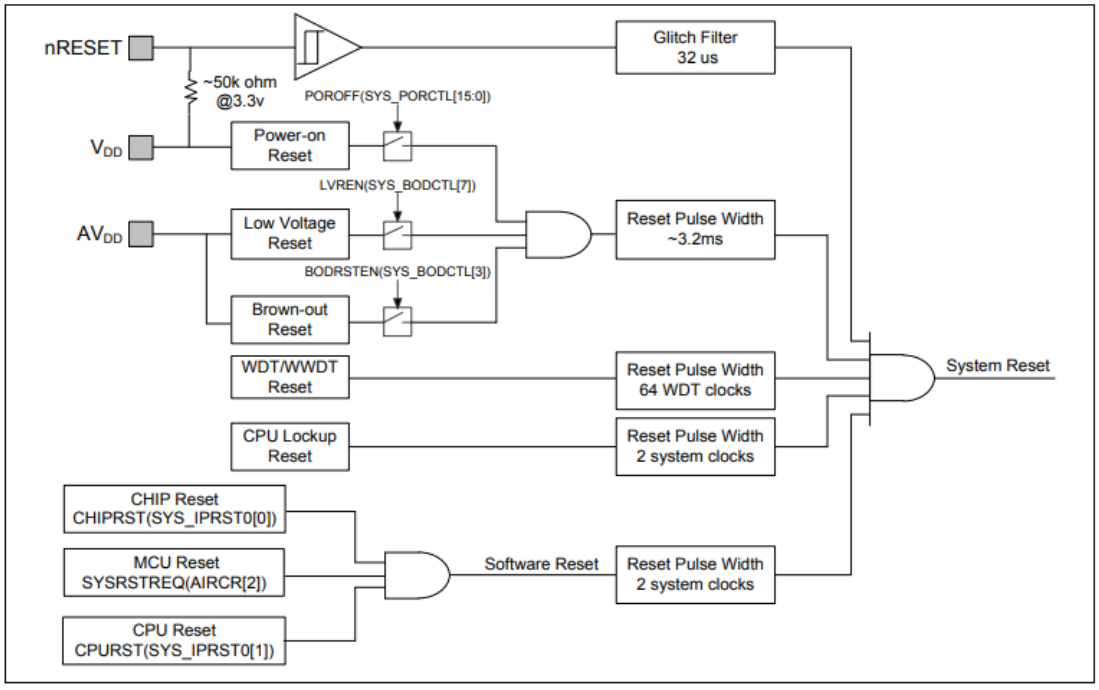


Figure 4.2-1 System Reset Sources

There are a total of 9 reset sources in the family. In general, CPU reset is used to reset Cortex®-M4 only; the other reset sources will reset Cortex®-M4 and all peripherals. However, there are small differences between each reset source and they are listed in Table 4.2-1.

Reset Sources Register	POR	nRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	-
(CLK_CLKSEL0[2:0])	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-

WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1]) BL (FMC_ISPCTL[16])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-'means that the value of register keeps original setting.									

Table 4.2-1 Reset Value of Registers

4.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 VDD and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 VDD and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset Figure 4.2-2 shows the nRESET reset waveform.

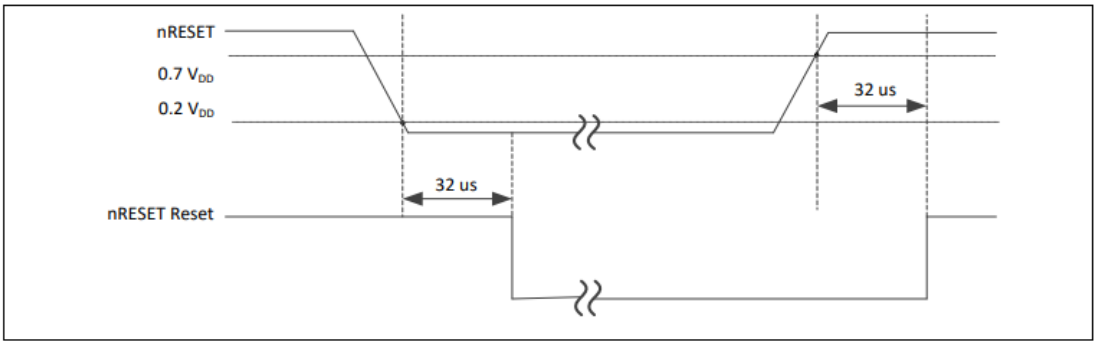


Figure 4.2-2 nRESET Reset Waveform

4.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

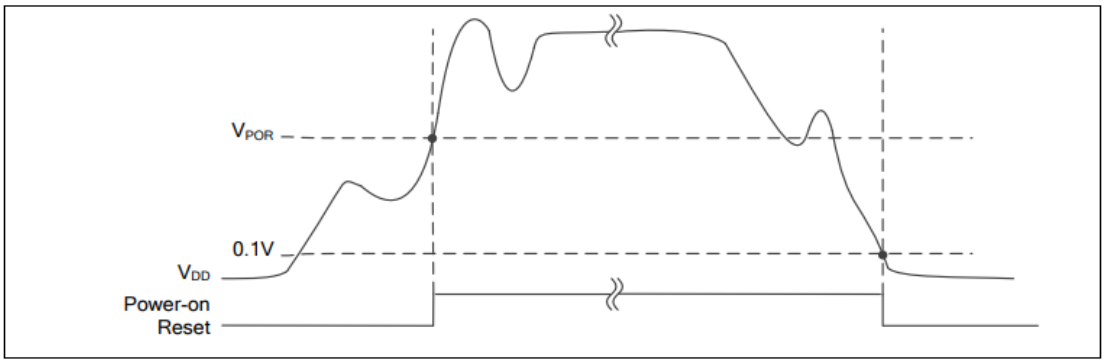


Figure 4.2-3 Power-on Reset (POR) Waveform

4.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AVDD during system operation. When the AVDD voltage is lower than VLVR and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AVDD voltage rises above VLVR and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 4.2-4 shows the

Low Voltage Reset waveform.

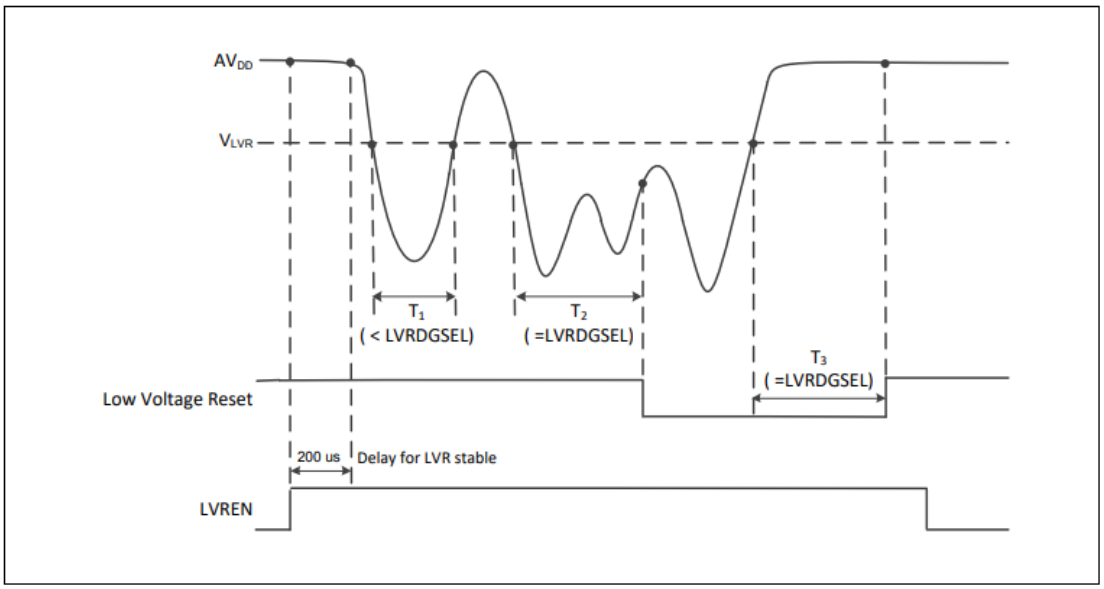


Figure 4.2-4 Low Voltage Reset (LVR) Waveform

4.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AVDD during system operation. When the AVDD voltage is lower than VBOD which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AVDD voltage rises above VBOD and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 4.2-5 shows the Brown-out Detector waveform.

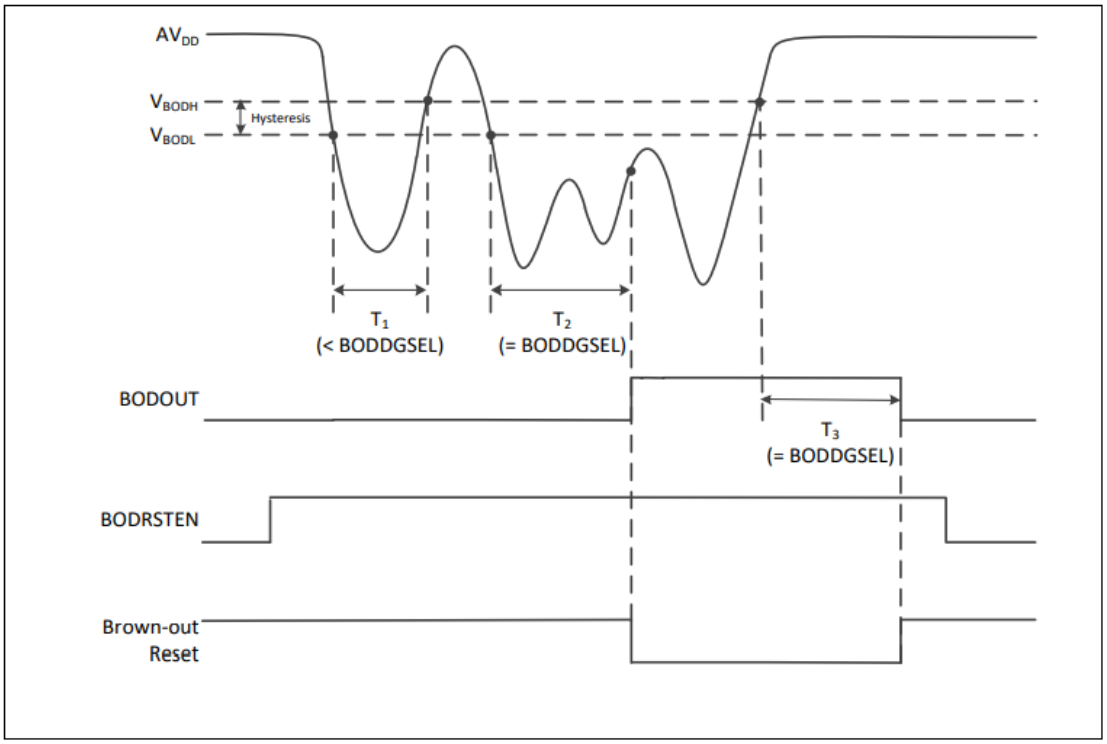


Figure 4.2-5 Brown-out Detector (BOD) Waveform

4.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

4.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor’s built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

4.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are

reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal. The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

4.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AVDD and AVSS provides the power for analog components operation.
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.
- RTC power from VBAT provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AVDD) should be the same voltage level of the digital power (VDD). Figure 4.2-6 shows the ITM-MV8 power distribution.

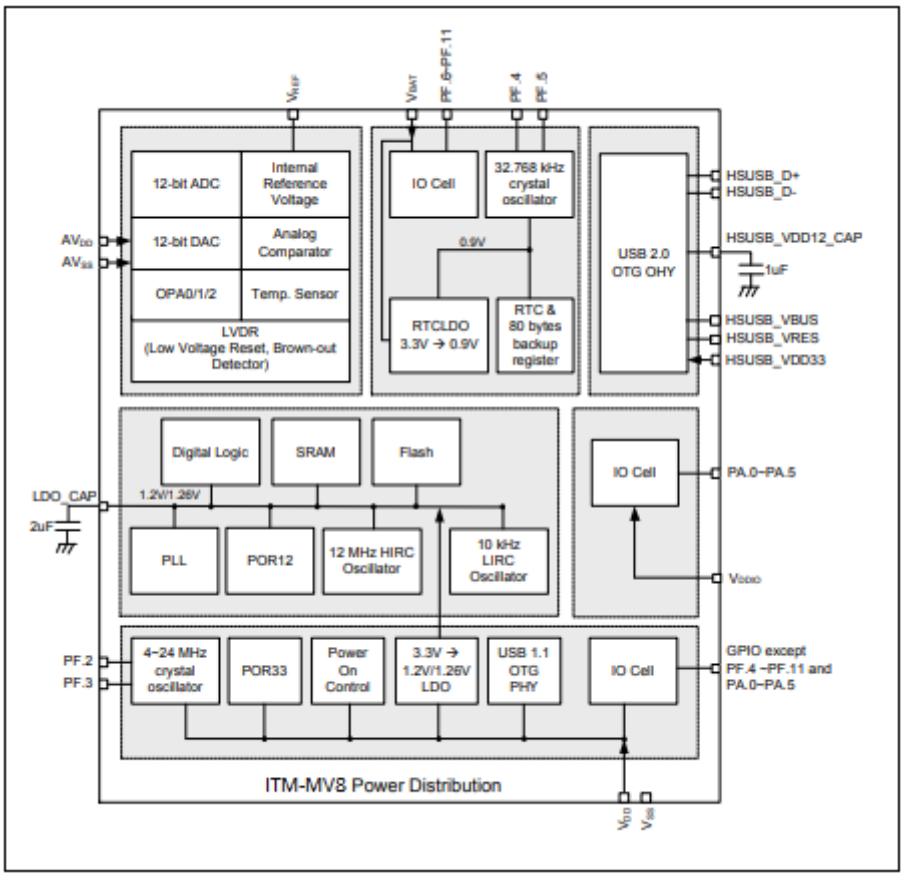


Figure 4.2-6 ITM-MV8-ANT Power Distribution Diagram

Note:

1. When VBAT power source first power-on, the power-on reset will happened and reset all VBAT domain circuit. The I/O in VBAT domain (PF.4 ~ PF.11) will become floating state and make additional leakage in VBAT domain. User should power on VDD first to reset chip and set I/O control to make these I/Os becomes a static state to prevent additional leakage.
2. The VBAT domain I/O (PF.4 ~ PF.11) will have unpredictable 1.5V glitch during power-on if VBAT and VDD connect together. To prevent this unpredictable glitch to make, user should avoid use these pins to be other IC's active or inactive control pins.

4.2.4 Power Modes and Wake-up Sources

The ITM-MV8 series has power manager unit to support several operating modes for saving power. Table 4.2-2 lists all power mode at ITM-MV8 series.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode	160	1.20	All clocks are disabled by control register.
Turbo mode	192	1.26	All clocks are disabled by control register.
Idle mode	CPU enter Sleep mode	1.20/1.26	Only CPU clock is disabled.
Fast Wakeup Power-down mode (FWPD)	CPU enters Deep Sleep mode	1.20/1.26	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Normal Power-down mode (NPD)	CPU enters Deep Sleep mode	1.20/1.26	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Low leakage Power-down mode (LLPD)	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Standby Power-down mode (SPD0)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage
Standby Power-down mode (SPD1)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage
Deep Power-down mode (DPD)*	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage

Table 4.2-2 Power Mode Table

Note:

1. User must turn on LIRC before entering SPD0/1 mode.
2. SPD0 mode has 32KB data retention in SRAM bank0.

There are different power mode entry setting for each power mode, they have different entry setting and leaving condition. Table 4.2-3 shows the entry setting for each power mode. When chip power-on, chip is running an normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT:[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction. And

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Fast Wakeup Power-down mode	1	1	2	YES
Normal Power-down mode	1	1	0	YES
Low leakage Power-down mode	1	1	1	YES
Standby Power-down mode 0	1	1	4	YES
Standby Power-down mode 1	1	1	5	YES
Deep Power-down mode*	1	1	6	YES

Table 4.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 4.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retender.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, USBD, ACMP and BOD.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 4.2-4 Power Mode Definition Table

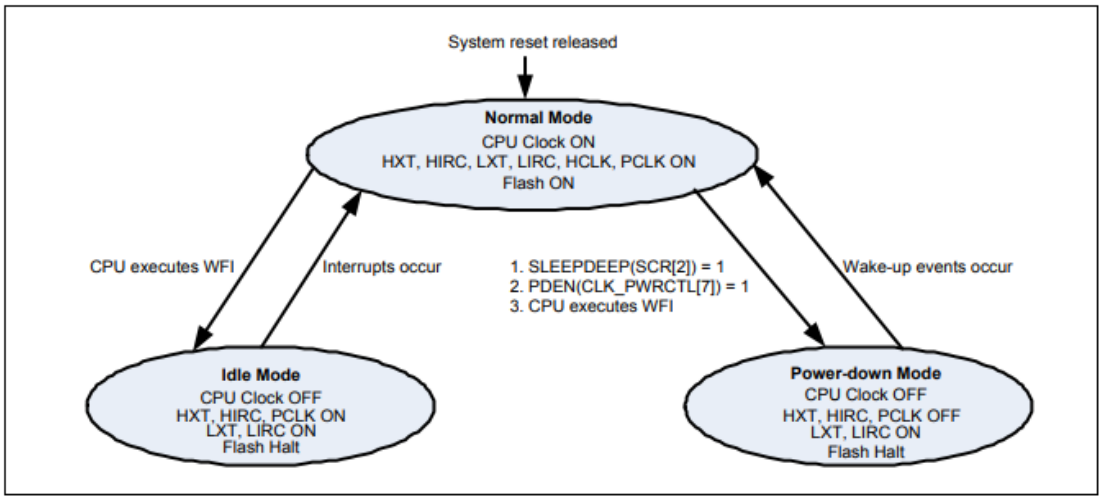


Figure 4.2-7 Power Mode State Machine

	Idle Mode	NPD, LLPD, FWPD	SPD	DPD
HXT	ON	Halt	Halt	Halt
HIRC	ON	Halt	Halt	Halt
LXT	ON	ON/OFF[1]	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON/OFF[2]	ON/OFF[2]	ON/OFF[2,8]
PLL	ON	Halt	Halt	Halt
HCLK/PCLK	ON	Halt	Halt	Halt
CPU	Halt	Halt	Halt	Halt
SRAM retention	ON	ON	ON/OFF[7]	Halt
FLASH	ON	Halt	Halt	Halt
TIMER	ON	ON/OFF[3]	ON/OFF[3]	Halt
WDT	ON	ON/OFF[4]	ON/OFF[4]	Halt
RTC	ON	ON/OFF[5]	ON/OFF[5]	ON/OFF[5]
UART	ON	ON/OFF[6]	ON/OFF[6]	Halt
Others	ON	Halt	Halt	Halt

Table 4.2-5 Clocks in Power Modes

Note:

1. LXT ON or OFF depends on SW setting in normal mode.
2. LIRC ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

7. SRAM retention size depends on SW setting in normal mode.
8. If timer wake up function is disabled, LIRC will be disabled automatically when chip enter DPD mode for power saving.

Wake-up sources in Normal Power-down mode (NPD):
RTC, WDT, I²C, Timer, UART, USCI, BOD, EBOD, GPIO, USBD, and ACMP.
After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 4.2-6 lists the condition about how to enter Power-down mode again for each peripheral.
User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	**Wake-Up Condition**	**Power-Down Mode**			**Re-Entering Power-Down Mode Condition**
		NPD/ FWPD/ LLPD	SPD	DPD	
BOD	Brown-Out Detector Reset / Interrupt	V	-	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-Out Detector Reset	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	-	-	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	V	V	-	After software writes 1 to clear PORF (SYS_RSTSTS[0])
INT	External Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PA~PD) Wake-up pin	rising or falling edge event, 64-pin	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear GPxWK (CLK_PMUSTS[11:8]) when SPD mode is entered.
GPIO(PC.0) Wake-up pin	rising or falling edge event , 1-pin	-	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear PINWK0 (CLK_PMUSTS[0]) when DPD mode is entered.

GPIO(PC.0/PB.0/PB.2/PB.12/PF.6) Wake-up pin	rising or falling edge event, 5-pin	-	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear PINWKx (CLK_PMUSTS[6:3] and CLK_PMUSTS[0]) when DPD mode is entered.
TIMER	Timer Interrupt	V	-	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	V	-	-	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	V	-	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	-	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
UART	nCTS wake-up	V	-	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	-	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	-	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	-	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	-	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	V	-	-	After software writes 1 to clear WKF (UI^2C_WKSTS[0]).
	Address match	V	-	-	After software writes 1 to clear WKAKDONE (UI^2C_PROTSTS[16], then writes 1 to clear WKF (UI^2C_WKSTS[0]).

USCI SPI	SS Toggle	V	-	-	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	V	-	-	After software writes 1 to clear WKAKDONE (I^2C_WKSTS[1]). Then software writes 1 to clear WKIF(I^2C_WKSTS[0]).
USBD	Remote Wake-up	V	-	-	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	V	-	-	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
ACMP	ACMPO status change	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear ACMPWK (CLK_PMUSTS[14]) when SPD mode is entered.

Table 4.2-6 Re-Entering Power-down Mode Condition

4.2.5 Power Modes and Power Level Transition

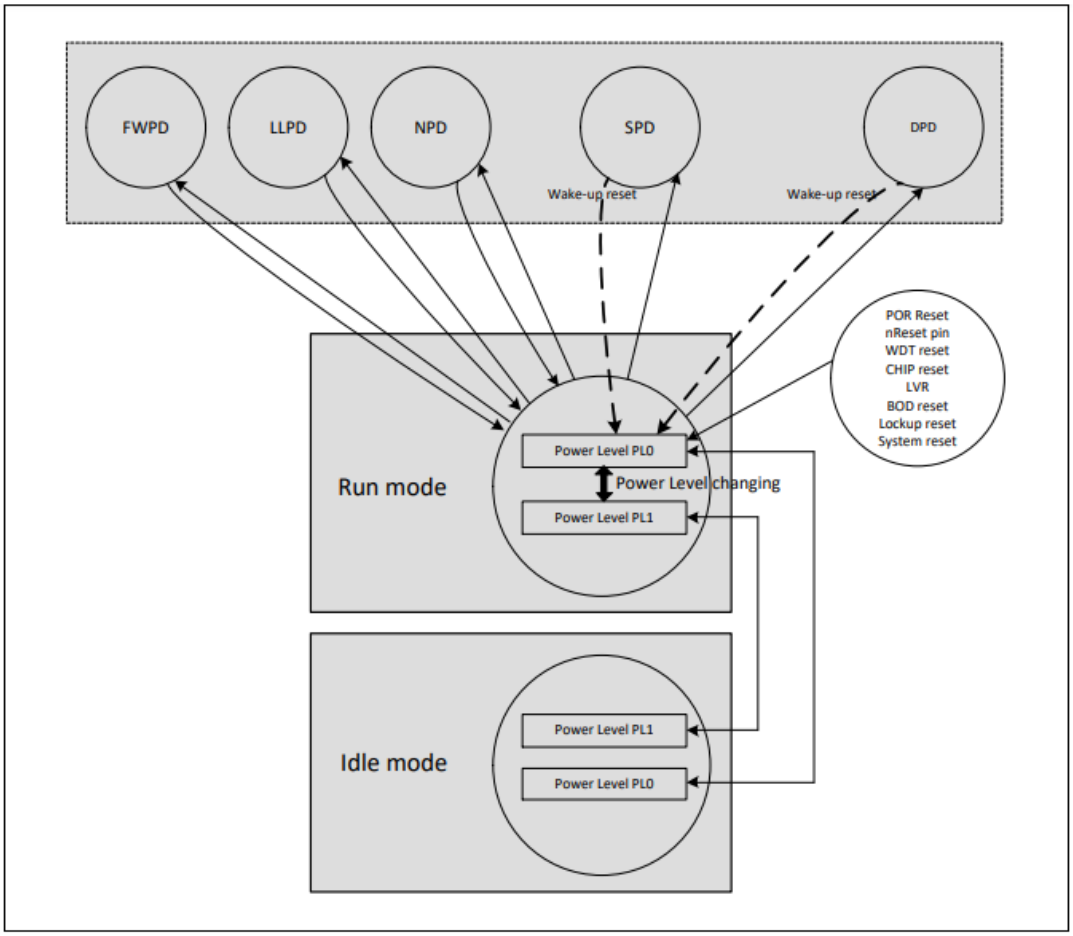


Figure 4.2-8 ITM-MV8-ANT Power Distribution Diagram

4.2.6 System Memory Map

The ITM-MV8 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 4.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The ITM-MV8 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 Kbytes)
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH Memory Space (512 Kbytes)
0x0800_0000 – 0x09FF_FFFF	SPIM_BA	SPIM Memory Space (32 Mbytes)
0x2000_0000 – 0x2000_7FFF	SRAM0_BA	SRAM Memory Space (32 Kbytes)
0x2000_8000 – 0x2001_FFFF	SRAM1_BA	SRAM Memory Space (96 Kbytes)
0x2002_0000 – 0x2002_7FFF	SRAM2_BA	SRAM Memory Space (32 Kbytes) for CPU only and share with SPIM cache
0x6000_0000 – 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (256 Mbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_7000 – 0x4000_7FFF	SPIM_BA	SPIM Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4000_D000 – 0x4000_DFFF	SDH0_BA	SDHOST0 Control Registers
0x4000_E000 – 0x4000_EFFF	SDH1_BA	SDHOST1 Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4001_9000 – 0x4001_9FFF	HSUSBD_BA	HSUSBD Control Registers
0x4001_A000 – 0x4001_AFFF	HSUSBH _BA	HSUSBH Host Control Registers
0x4003_0000 – 0x4003_0FFF	CCAP_BA	CCAP Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
0x4003_E000 – 0x4003_EFFF	SWDC_BA	SWD Control Registers
0x4003_F000 – 0x4003_FFFF	ETMC_BA	ETM Control Registers

0x5008_0000 – 0x5008_0FFF	CRYP_BA	Cryptographic Accelerator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4004_6000 – 0x4004_6FFF	OPA_BA	OP Amplifier Control Registers
0x4004_7000 – 0x4004_7FFF	DAC_BA	DAC Control Registers
0x4004_B000 – 0x4004_BFFF	EADC1_BA	Enhanced Analog-Digital-Converter 1 (EADC1) Control Registers
0x4004_D000 – 0x4004_DFFF	OTG_BA	OTG Control Registers
0x4004_F000 – 0x4004_FFFF	HSOTG_BA	HSOTG Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	EPWM1_BA	EPWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	QSPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4006_3000 – 0x4006_3FFF	SPI2_BA	SPI2 Control Registers
0x4006_4000 – 0x4006_4FFF	SPI3_BA	SPI3 Control Registers
0x4006_9000 – 0x4006_9FFF	QSPI1_BA	QSPI1 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4007_6000 – 0x4007_6FFF	UART6_BA	UART6 Control Registers
0x4007_7000 – 0x4007_7FFF	UART7_BA	UART7 Control Registers
0x4008_0000 – 0x4008_0FFF	I^2C0_BA	I^2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I^2C1_BA	I^2C1 Control Registers
0x4008_2000 – 0x4008_2FFF	I^2C2_BA	I^2C2 Control Registers
0x4009_0000 – 0x4009_0FFF	SC0_BA	Smartcard Host 0 Control Registers

0x4009_1000 – 0x4009_1FFF	SC1_BA	Smartcard Host 1 Control Registers
0x4009_2000 – 0x4009_2FFF	SC2_BA	Smartcard Host 2 Control Registers
0x4009_3000 – 0x4009_3FFF	SC3_BA	Smartcard Host 3 Control Registers
0x400B_0000 – 0x400B_0FFF	QEI0_BA	QEI0 Control Registers
0x400B_1000 – 0x400B_1FFF	QEI1_BA	QEI1 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400B_5000 – 0x400B_5FFF	ECAP1_BA	ECAP1 Control Registers
0x400B_9000 – 0x400B_9FFF	TRNG_BA	TRNG Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

4.2.7 SRAM Memory Organization

The ITM-MV8 series supports embedded SRAM with total 160 Kbytes size and the SRAM organization is separated to three banks: SRAM bank0 and SRAM bank1 and SRAM bank2. The first bank has 32 Kbytes address space, the second bank has 96 Kbyte address space and the third bank has 32Kbyte. These three banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure chip operating more stable. The SRAM bank2 is shared with SPIM cache, it can switch to external SPI Flash cache memory. Note that SRAM bank2 has additional two wait cycles when reading data.

- Supports total 160 Kbytes SRAM
- Supports byte / half word / word write
- Supports fixed 32 Kbytes SRAM bank0 for independent access
- Supports parity error check function for SRAM bank0
- Supports oversize response error
- Supports remap address to 0x1000_0000

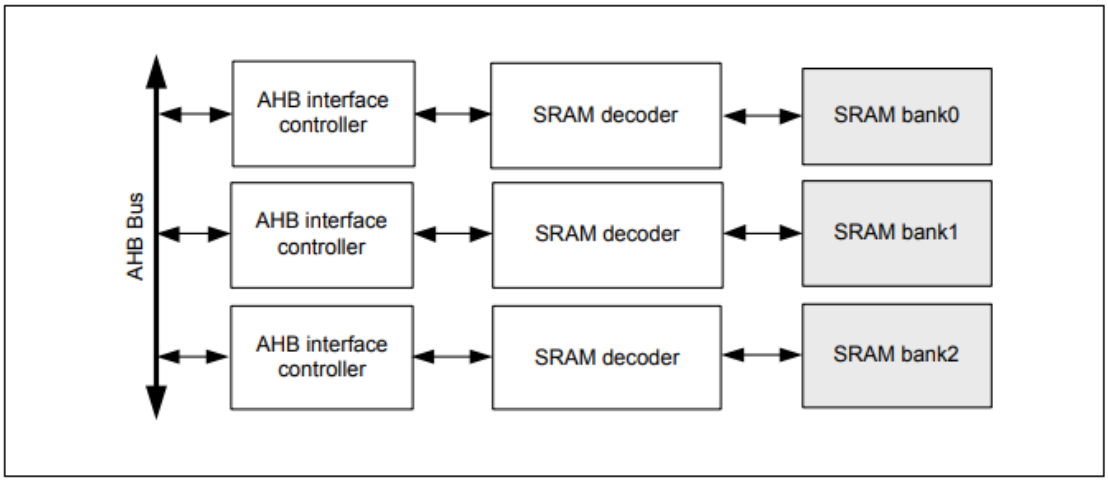


Figure 4.2-9 SRAM Block Diagram

Figure 4.2-9 shows the SRAM organization of ITM-MV8-ANT. There are three SRAM banks in ITM-MV8-ANT. The bank0 is addressed to 32 Kbytes, the bank1 is addressed to 96 Kbytes and the bank2 is addressed to 32 Kbyte. The bank0 address space is from 0x2000_0000 to 0x2000_7FFF. The bank1 address space is from 0x2000_8000 to 0x2001_FFFF. The bank2 address space is from 0x2002_0000 to 0x2002_7FFF. The address between 0x2002_8000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

	160 Kbytes Device	**128 Kbytes Device**	**64KB Device**	**Read Access**
SRAM bank0	0x2000_0000 ~ 0x2000_7FFF or 0x1000_0000 ~ 0x1000_7FFF	0x2000_0000 ~ 0x2000_7FFF or 0x1000_0000 ~ 0x1000_7FFF	0x2000_0000 ~ 0x2000_7FFF or 0x1000_0000 ~ 0x1000_7FFF	Zero wait cycle for continuous access
SRAM bank1	0x2000_8000 ~ 0x2001_FFFF or 0x1000_8000 ~ 0x1001_FFFF	0x2000_8000 ~ 0x2001_FFFF or 0x1000_8000 ~ 0x1001_FFFF	0x2000_8000 ~ 0x2000_FFFF or 0x1000_8000 ~ 0x1000_FFFF	Zero wait cycle for continuous access
SRAM bank2	0x2002_0000 ~ 0x2002_7FFF or 0x1002_0000 ~ 0x1002_7FFF			Two wait cycles

Table 4.2-8 SRAM Organization

The address of each bank is remapping from 0x2000_0000 to 0x1000_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_7FFF or 0x1000_0000 to

0x1000_7FFF, and access SRAM bank1 through 0x2000_8000 to 0x2001_FFFF or 0x1000_8000 to 0x1001_FFFF, and access SRAM bank2 through 0x2002_0000 to 0x2002_7FFF or 0x1002_0000 to 0x1002_7FFF.

When setting the control register CCMEN(SPIM_CTL1[2]) to 0, SRAM bank2 is switched to external SPI Flash cache memory. In this case, the SRAM bank2 can't be accessed as general SRAM. If user access SRAM bank2 by AHB bus master, the SPI Flash controller will send error response via HRESP AHB bus signal to bus master.

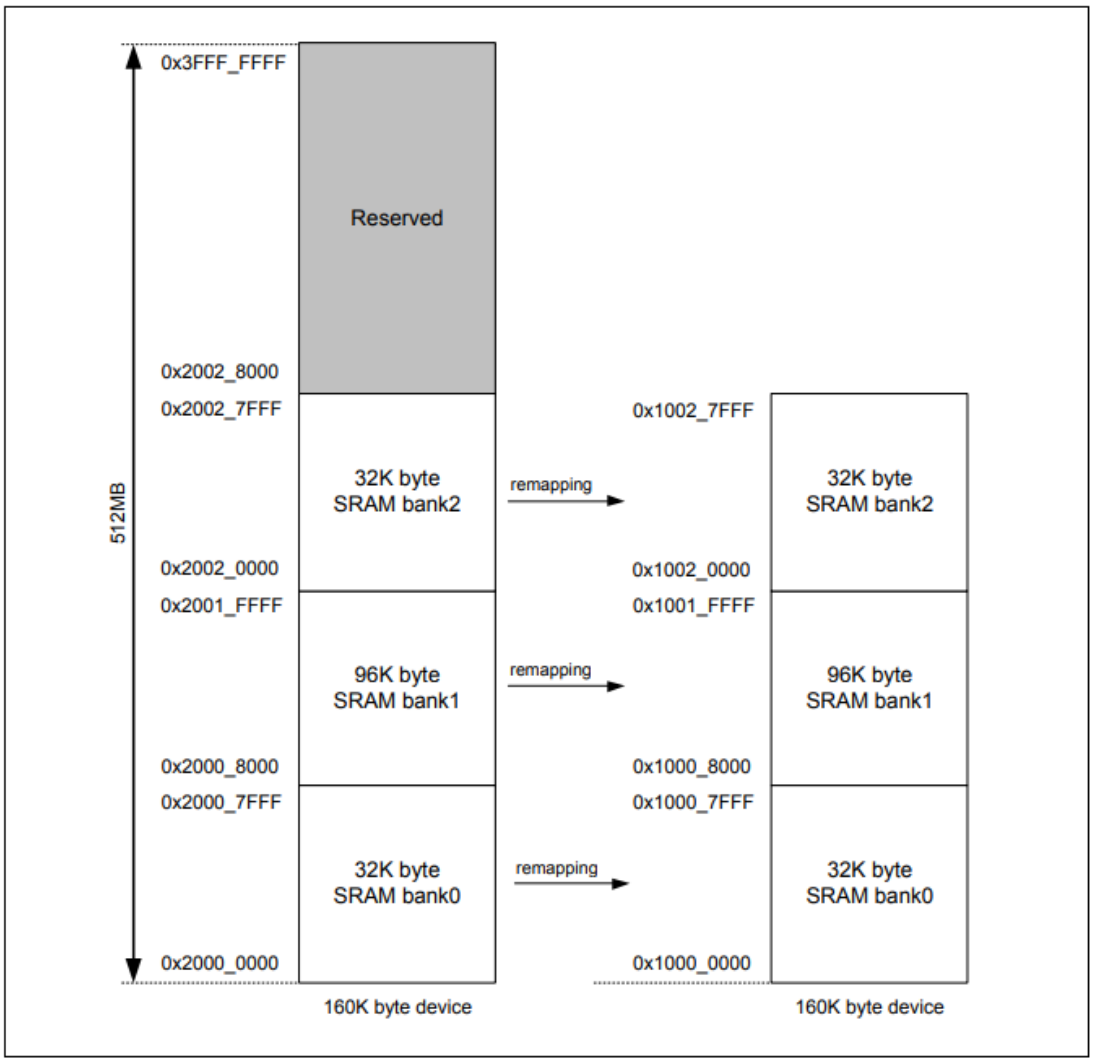


Figure 4.2-10 SRAM Memory Organization

SRAM bank0 has byte parity error check function. When CPU is accessing SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occurred, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occurred, chip will stop detecting SRAM parity

error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

4.2.8 HIRC Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator) and HIRC trim (48 MHz RC oscillator,), according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 12 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

4.2.9 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

SYS_IPRST0	**Address 0x4000_0008**
SYS_BODCTL	address 0x4000_0018
SYS_VREFCTL	address 0x4000_0028
SYS_USBPHY	address 0x4000_002C
SYS_SRAM_BISTCTL	address 0x4000_00D0
SYS_PORDISAN	address 0x4000_01EC

SYS_PLCTL	address 0x4000_01F8
CLK_PWRCTL	address 0x4000_0200
CLK_APBCLK0	address 0x4000_0208
CLK_CLKSEL0	address 0x4000_0210
CLK_CLKSEL1	address 0x4000_0214
CLK_PLLCTL	address 0x4000_0240
CLK_PMUCTL	address 0x4000_0290
NMIEN	address 0x4000_0300
AHBMCTL	address 0x4000_0400
FMC_FTCTL	address 0x4000_5018
FMC_ICPCMD	address 0x4000_501C
FMC_ISPCTL	address 0x4000_C000
FMC_ISPTRG	address 0x4000_C010
FMC_ISPSTS	address 0x4000_C040
FMC_CYCCTL	address 0x4000_C04C
FMC_KPKEYTRG	address 0x4000_C05C
FMC_KPKEYSTS	address 0x4000_C060
WDT_CTL	address 0x4004_0000
WDT_ALTCTL	address 0x4004_0004
TIMER0_CTL	address 0x4005_0000
TIMER1_CTL	address 0x4005_0100
TIMER2_CTL	address 0x4005_1000
TIMER3_CTL	address 0x4005_1100
TIMER0_PWMCTL	address 0x4005_0040
TIMER1_PWMCTL	address 0x4005_0140
TIMER2_PWMCTL	address 0x4005_1040
TIMER3_PWMCTL	address 0x4005_1140
TIMER0_PWMDTCTL	address 0x4005_0058
TIMER1_PWMDTCTL	address 0x4005_0158
TIMER2_PWMDTCTL	address 0x4005_1058
TIMER3_PWMDTCTL	address 0x4005_1158
TIMER0_PWMBRKCTL	address 0x4005_0070
TIMER1_PWMBRKCTL	address 0x4005_0170
TIMER2_PWMBRKCTL	address 0x4005_1070
TIMER3_PWMBRKCTL	address 0x4005_1170

TIMER0_PWMSWBRK	address 0x4005_007C
TIMER1_PWMSWBRK	address 0x4005_017C
TIMER2_PWMSWBRK	address 0x4005_107C
TIMER3_PWMSWBRK	address 0x4005_117C
TIMER0_PWMINTEN1	address 0x4005_0084
TIMER1_PWMINTEN1	address 0x4005_0184
TIMER2_PWMINTEN1	address 0x4005_1084
TIMER3_PWMINTEN1	address 0x4005_1184
TIMER0_PWMINTSTS1	address 0x4005_008C
TIMER1_PWMINTSTS1	address 0x4005_018C
TIMER2_PWMINTSTS1	address 0x4005_108C
TIMER3_PWMINTSTS1	address 0x4005_118C
EPWM_CTL0	address 0x4005_8000/0x4005_9000
EPWM_CTL1	address 0x4005_8000/0x4005_9000
EPWM_DTCTL0_1	address 0x4005_8070/0x4005_9070
EPWM_DTCTL2_3	address 0x4005_8074/0x4005_9074
EPWM_DTCTL4_5	address 0x4005_8078/0x4005_9078
EPWM_BRKCTL0_1	address 0x4005_80C8/0x4005_90C8
EPWM_BRKCTL2_3	address 0x4005_80CC/0x4005_90CC
EPWM_BRKCTL4_5	address 0x4005_80D0/0x4005_90D0
EPWM_SWBRK	address 0x4005_80DC/0x4005_90DC
EPWM_INTEN1	address 0x4005_80E4/0x4005_90E4
EPWM_INTSTS1	address 0x4005_80EC/0x4005_90EC
BPWM_CTL0	address 0x4005_A000/0x4005_B000
SYST_VAL	address 0xE000_E018

4.2.10 System Timer (SysTick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear- on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.
If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.
For more detailed information, please refer to the “Arm® Cortex® -M4 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”.

4.2.11 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.
The NVIC supports:

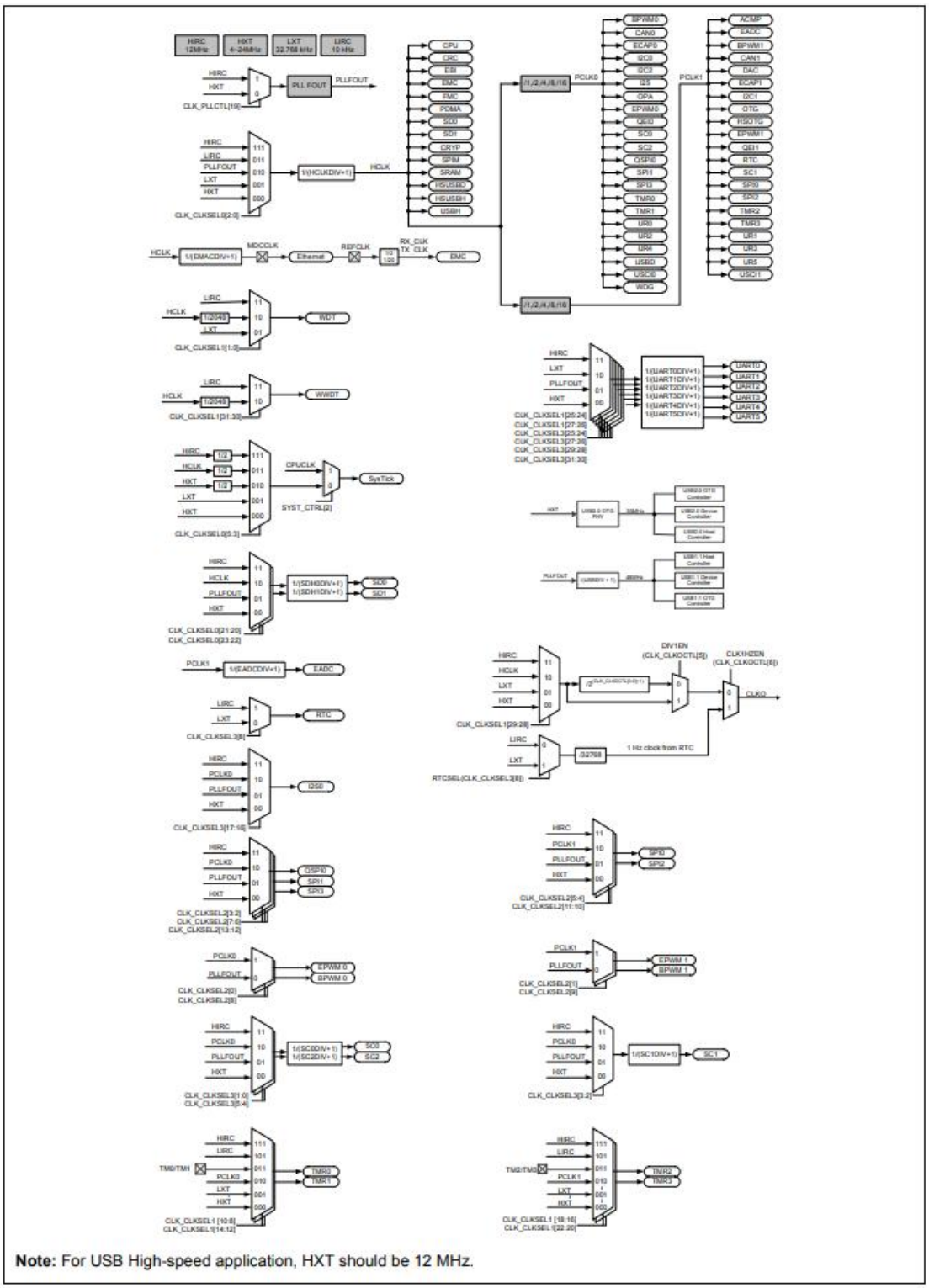
- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

4.3 Clock Controller

4.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M4F core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 12 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 4.3-1 shows the clock generator and the overview of the clock source control.



Note: For USB High-speed application, HXT should be 12 MHz.

Figure 4.3-1 Clock Generator Global View Diagram (ITM-MV8-ANT)

4.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- 12 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

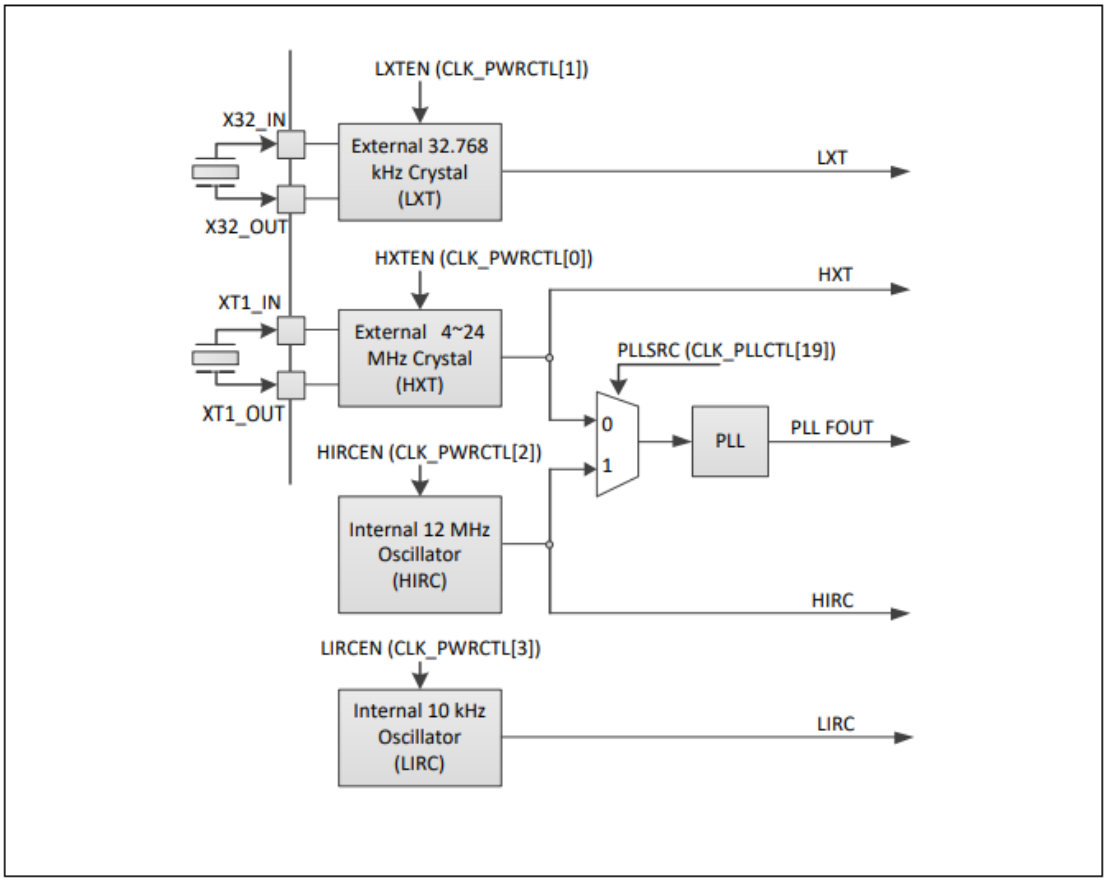


Figure 4.3-3 Clock Generator Block Diagram

4.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 4.3-4.

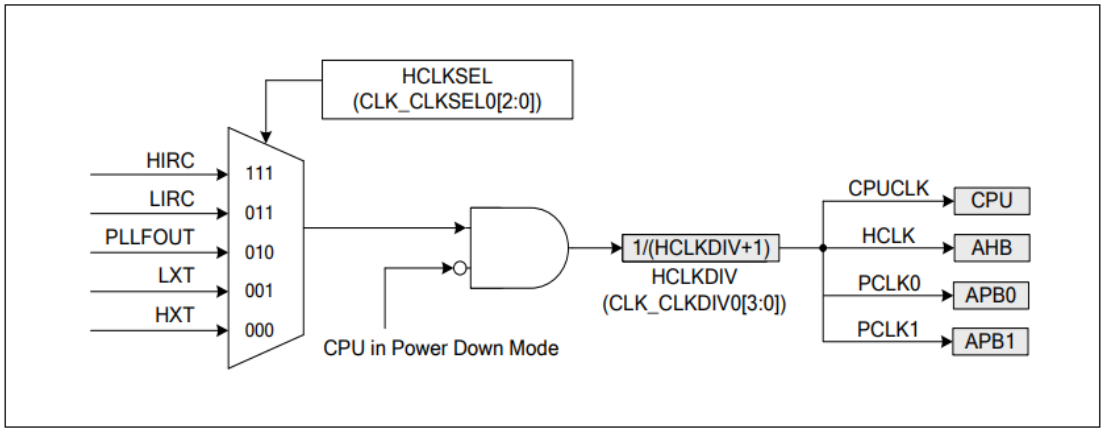


Figure 4.3-4 System Clock Block Diagrams

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 4.3-5 shows The HXT clock stops detection and system clock switches to HIRC procedure

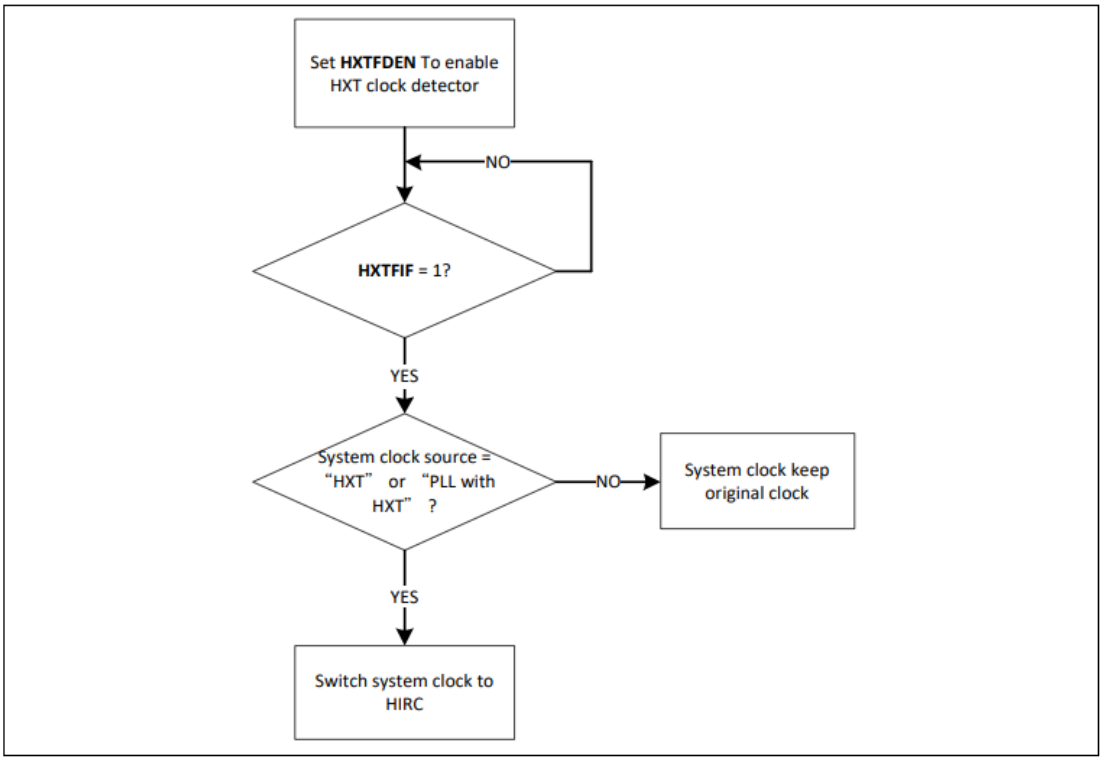


Figure 4.3-5 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M4F core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 4.3-6.

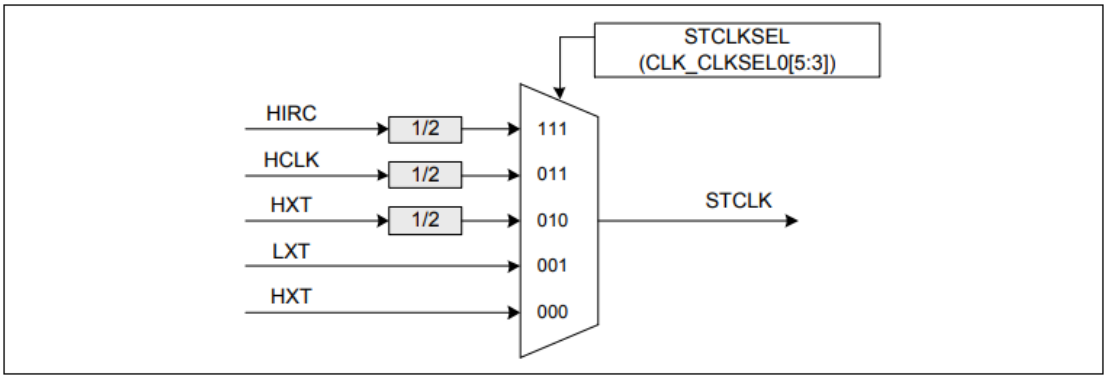


Figure 4.3-6 SysTick Clock Control Block Diagram

4.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register.

4.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

4.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide- by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from Fin/21 to Fin/216 where Fin is input clock frequency to the clock divider.

The output formula is Fout = Fin/2(N+1), where Fin is the input clock frequency, Fout is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count.

When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

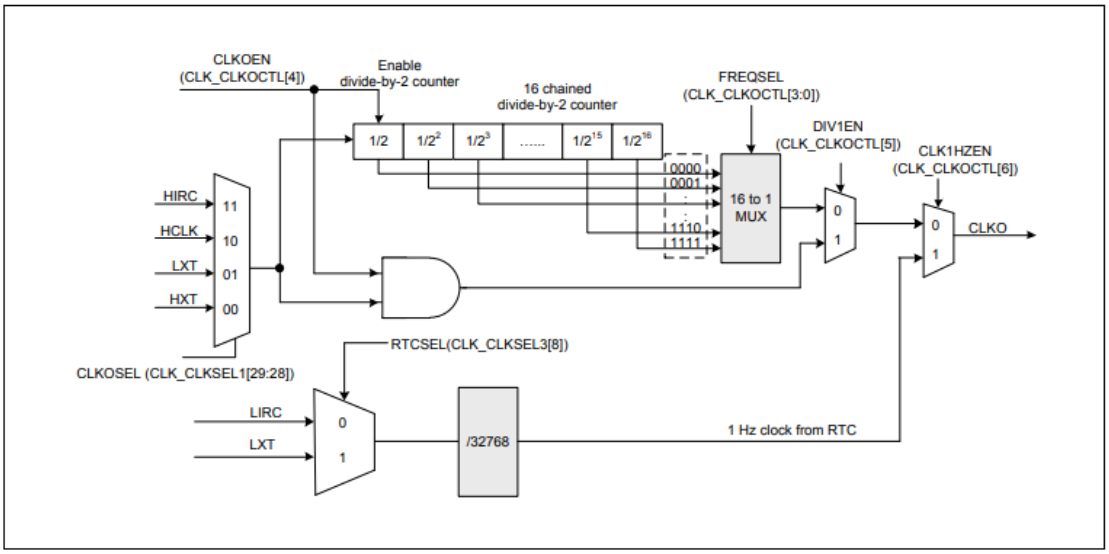


Figure 4.3-7 Clock Output Block Diagram

4.4 True Random Number Generator (TRNG)

4.4.1 Overview

The True Random Number Generator (TRNG) is used to generate the randomness by extracting from physical phenomena.

4.4.2 Features

Generates 800 random bits per second

4.5 Flash Memory Controller (FMC)

4.5.1 Overview

The FMC is equipped with 128/256/512 Kbytes on-chip embedded Flash for application and configurable Data Flash to store some application dependent data. Thus, the total size of application rom (APROM) is 128/256/512 Kbytes. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 4 Kbytes security protection ROM (SPROM) can conceal user program. A 3 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data. A 32 Kbytes Boot Loader consists of native ISP functions and secure boot function. A 8 Kbytes Boot Loader consists of secure boot function. A 4 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In- Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

4.5.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports 512 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 4 Kbytes security protection ROM (SPROM) to conceal user program
- Supports mirror SPROM in dual-bank Flash macro to read SPROM code while writing other ROM
- Supports 4 XOM (eXecution Only Memory) regions to conceal user program in APROM.
- Supports Data Flash with configurable memory size
- Supports 16 bytes User Configuration block to control system initiation

- Supports 3 Kbytes one-time-program ROM (OTP)
- Supports 4 Kbytes page erase for all embedded Flash
- Supports block and bank erase for APROM, except for XOM regions
- Supports Boot Loader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for code integrity and authenticity
- Supports Security Key protection function for APROM, LDROM, SPROM, User Configuration block and KPROM protection
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption
- Supports auto-tuning Flash access cycle function to optimize the Flash access performance

FMC Features	**ITM-MV8**
Dual-bank Flash macro	•
512 Kbytes APROM	•
4 Kbytes LDROM	•
4 Kbytes SPROM	•
Data Flash with configurable memory size	•
16 bytes User Configuration block (UCFG)	•
3 Kbytes OTP	•
8 Kbytes KPROM	•
4 Kbytes page erase	•
Block and bank erase for APROM, except for XOM	•
32 Kbytes Boot Loader with native ISP functions	•
AES secure boot function	•
Security Key protection function for APROM and LDROM	•
Security Key protection function for UCFG and KPROM	•
Security Key protection function for SPROM	•
32-bit/64-bit and multi-word Flash programming function	•

Fast Flash programming verification function	•
CRC32 checksum calculation function	•
4 Kbytes cache memory	•
In-Application-Programming function (IAP)	•
Boot from boot loader via PF.0 at reset rising	•

Table 4.5-1 FMC Features Comparison Table at Different Chip

4.6 General Purpose I/O (GPIO)

4.6.1 Overview

This chip has up to 118 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 118 pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA, PB, PE and PG has 16 pins on port. PC, PD has 15 pins on port. PF, PH has 12 pins on port. Each of the 118 pins is independent and has the corresponding register bits to control the pin mode function and data.
The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

4.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function

4.7 PDMA Controller (PDMA)

4.7.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

4.7.2 Features

- Supports 16 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, DAC, ADC and PWM request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1
- Supports stride function from channel 0 to channel 5

4.8 Timer Controller (TMR)

4.8.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.
The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

4.8.2 Features

4.8.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, BPWM, QEI, EADC, DAC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports Inter-Timer trigger mode
- Supports event counting source from internal USB SOF signal

4.8.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake status cleared
  - Level detect brake source to auto recover function after brake condition

removed

- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
  - Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

4.9 Watchdog Timer (WDT)

4.9.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

4.9.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (24 ~ 218) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz or LXT.

4.10 Window Watchdog Timer (WWDT)

4.10.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

4.10.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

4.11 Real Time Clock (RTC)

4.11.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

4.11.2 Features

- Supports independent RTC power domain with external power pin V BAT.
- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.

- Supports up to 6 individual tamper pins.
- Supports 20/80 bytes spare registers and tamper pins detection to clear the content of these spare registers.

4.12 EPWM Generator and Capture Timer (EPWM)

4.12.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

4.12.2 Features

4.12.2.1 EPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period

- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter matches free trigger comparator compared value (only for EADC)
- Supports EPWM trigger EADC event prescaler feature

4.12.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

4.13 Basic PWM Generator and Capture Timer (BPWM)

4.13.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC0/1 to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

4.13.2 Features

4.13.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC0/1 in the following events:
  - BPWM counter matches 0, period value or compared value

4.13.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

	ITM-MV8
Trigger numbers for EADC	1

Table 4.13-1 BPWM Features Comparison Table

4.14 Quadrature Encoder Interface (QEI)

4.14.1 Overview

There are two QEI controllers in this device. The Quadrature Encoder Interface (QEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

4.14.2 Features

4.14.2.1 Quadrature Encoder Interface (QEI) Features

- Up to two QEI controllers, QEI0 and QEI1.
- Two QEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (QEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (QEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (QEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (QEI_CNTCMP) with a Pre-set Maximum Count Register (QEI_CNTMAX)
- One QEI control register (QEI_CTL) and one QEI Status Register (QEI_STATUS)
- Four Quadrature encoder pulse counter operation modes
  - Support x4 free-counting mode
  - Support x2 free-counting mode
  - Support x4 compare-counting mode
  - Support x2 compare-counting mode
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clk/8

4.15 Enhanced Input Capture Timer (ECAP)

4.15.1 Overview

The chip provides up to two units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

4.15.2 Features

- Up to two Input Capture Timer/Counter units, CAP0 and CAP1.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

4.16 UART Interface Controller (UART)

4.16.1 Overview

The chip provides three channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel- to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

4.16.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads

- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0/UART1 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode.

UART Feature	UART0/UART1	UART2 ~ UART7	SC_UART	USCI-UART
FIFO	16 Bytes	16 Bytes	4 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	-	√
IrDA	√	√	-	-
LIN	√	-	-	-
RS-485 Function Mode	√	√	-	√

nCTS Wake-up	√	√	-	√
Incoming Data Wake-up	√	√	-	√
Received Data FIFO reached threshold Wake-up	√	√	-	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-	-
Auto-Baud Rate Measurement	√	√	-	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√	√
Stick Bit	√	√	-	-
Note: √= Supported				

Table 4.16-1 ITM-MV8 Series UART Features

4.17 Serial Peripheral Interface (SPI)

4.17.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer.

4.17.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 96 MHz (when chip works at VDD = 2.7~3.6V)
  - Slave mode up to 96 MHz when SPI master device supports adjustment function of RX data sampling clock (when chip works at VDD = 2.7~3.6V)
  - Slave mode up to 48 MHz when SPI master device does not support adjustment function of RX data sampling clock (when chip works at VDD = 2.7~3.6V)
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers

- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports one data channel half-duplex transfer
- Supports receive-only mode

4.18 Quad Serial Peripheral Interface (QSPI)

4.18.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.
The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

4.18.2 Features

- Supports Master or Slave mode operation
- Master mode up to 96 MHz (when chip works at VDD = 2.7V~3.6V)
- Slave mode up to 96 MHz when SPI master device supports adjustment function of RX data sampling clock (when chip works at VDD = 2.7V~3.6V)
- Slave mode up to 48 MHz when SPI master device does not support adjustment function of RX data sampling clock (when chip works at VDD = 2.7V~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

4.19 SPI Synchronous Serial Interface Controller (SPI Master mode)

4.19.1 Overview

The SPI Synchronous serial Interface Controller for SPI master mode performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data received from MCU. This SPI controller can drive one external peripheral (External SPI Flash) and it is seen as the SPI master mode. It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The active level of device/slave select signal can be chosen to low active or high active, which depends on the peripheral. Writing a divisor into the SPIM_CTL1 register can program the frequency of serial clock output to the peripheral.

In SPI Flash controller, normal I/O mode contains four 32-bit transmit/receive buffers, and can provide 1 to 4 burst mode operation. The number of bits in each transaction can be 8, 16, 24, or 32; data can be transmitted/received up to four successive transactions in one transfer.

By DMA write mode, user can move data from SRAM to external SPI Flash component. In DMA read mode, user can move data from external SPI Flash component to SRAM.

In direct memory mapping mode (DMM mode), this SPI Flash controller will translate the AHB bus commands into SPI Flash operations without MCU setting related SPI Flash command. Therefore users can access external SPI Flash as a ROM module.

In direct memory mapping mode with cache off mode, it will pre-fetch 4-word Flash data after a direct memory mapping access. when using direct memory mapping mode with cache on mode, it will use 32 Kbytes cache memory to reduce the number of accessing external SPI Flash component and the performance of SPI Flash access can be improved. To improve the read operation of SPI Flash without increasing the serial clock frequency, this SPI Flash controller supports DTR/DDR (Double Transfer Rate/Double Data Rate) read command codes that support Standard/Dual/Quad SPI modes. The one byte command code is still latched into the device on the rising edge of the serial clock similar to all other SPI commands. Once a DTR/DDR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

In core coupled memory mode (CCM mode), the cache function is disabled by hardware automatically, and MCU can access this 32 Kbytes cache memory as general SRAM. For data protection, this SPI Flash controller supports cipher encryption and decryption circuits to protect data which user places into external SPI

Flash when DMA read/write mode and direct memory mapping mode are used.

4.19.2 Features

- Supports maximum 32 Mbytes SPI Flash size
- Supports SPI master mode
- Supports Direct Memory Mapping Mode and Normal I/O Mode
- Supports 8/16/24/32 bits transaction for Normal I/O mode
- Provides burst mode operation in Normal I/O mode, which can transmit/receive data up to four successive transactions in one transfer
- Supports DMA mode read/write
- Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
- Supports Double Transfer Rate (DTR) / Double Data Rate (DDR) transfer mode
- Supports 32 Kbytes cache memory
- Supports 32 Kbytes Core Coupled Memory (CCM) when cache function disable
- Supports Cipher encryption/decryption
- One slave/device select line for external SPI Flash component

4.20 I^2C Serial Interface Controller (I^2C)

4.20.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I^2C controllers which support Power-down wake-up function.

4.20.2 Features

The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I^2C bus include:

- Supports up to three I^2C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports High speed mode 3.4Mbps
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode

plus (1 Mbps)

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

4.21 USCI - Universal Serial Control Interface Controller (USCI)

4.21.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

4.21.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

4.22 USCI – UART Mode

4.22.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, and the transmission and reception can be started separately.

The UART controller also provides auto flow control. There are three conditions to wake up the system.

4.22.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA transfer
- Supports Wake-up function (Incoming Data and nCTS Wakeup Only)

4.23 USCI - SPI Mode

4.23.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

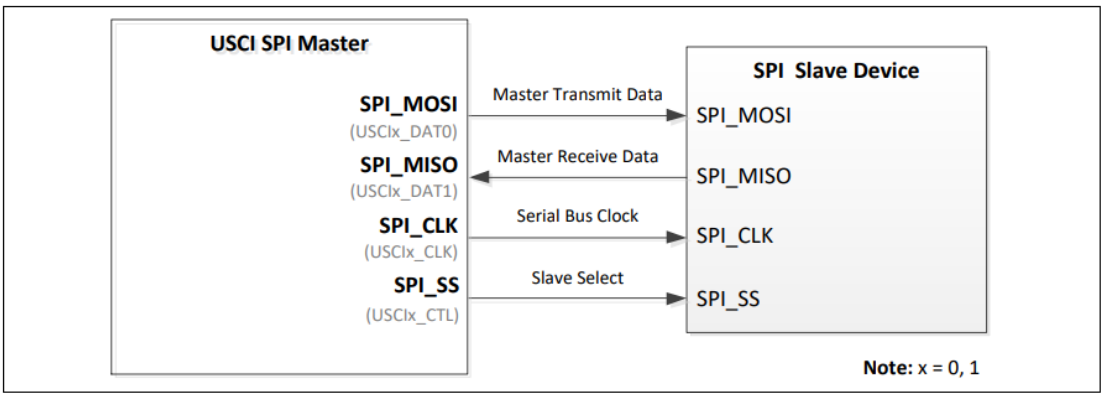


Figure 4.26-1 SPI Master Mode Application Block Diagram

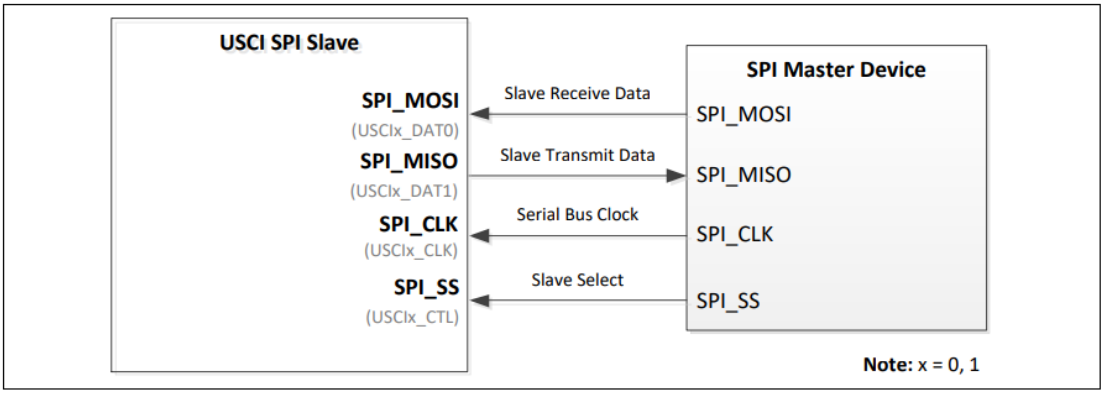


Figure 4.26-2 SPI Slave Mode Application Block Diagram

4.23.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = fPCLK / 2, Slave < fPCLK / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

4.24 USCI - I^{2}C Mode

4.24.1 Overview

On I^{2}C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 4.27-1 for more detailed I^{2}C BUS Timing.

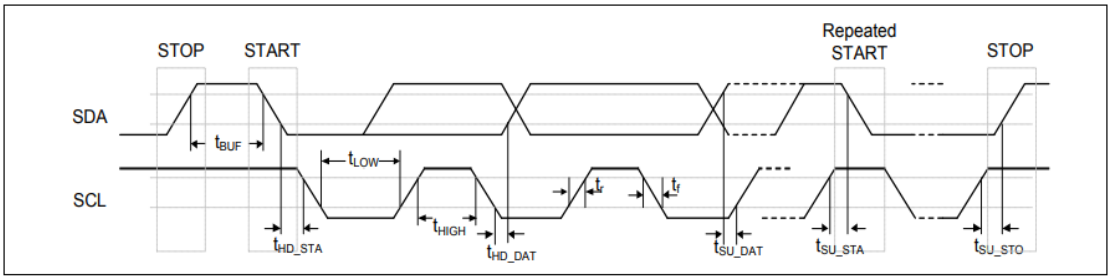


Figure 4.27-1 I^{2}C Bus Timing

The device's on-chip I^{2}C provides the serial interface that meets the I^{2}C bus standard mode specification. The I^{2}C port handles byte transfers autonomously. The I^{2}C mode is selected by FUNMODE (UI^{2}C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I^{2}C bus via two pins: SDA and SCL. When I/O pins are used as I^{2}C ports, user must set the pins function to I^{2}C in advance.

Note: Pull-up resistor is needed for I^{2}C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I^{2}C operation mode.

4.24.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by START signal or address match
- Supports setup/hold time programmable

- Supports multiple address recognition (two slave address with mask option)

4.25 USB 1.1 Device Controller (USBD)

4.25.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbytesytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug- in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to Universal Serial Bus Specification Revision 1.1.

4.25.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS)

- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbyte buffer size
- Provides remote wake-up capability

4.26 High Speed USB 2.0 Device Controller (HSUSBD)

4.26.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

4.26.2 Features

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint — Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 4092 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

4.27 CRC Controller (CRC)

4.27.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

4.27.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1’s complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

4.28 Enhanced 12-bit Analog-to-Digital Converter (EADC)

4.28.1 Overview

The chip contains one or two 12-bit successive approximation analog-to-digital converter (SAR EADC converter) with 16 external input channels and 3 internal channels. The EADC0/1 converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0/1_ST) input signal.

4.28.2 Features

- Analog input voltage range: 0~ VREF (Max to 3.6V)
- Reference voltage from VREF pin.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage (VBG), temperature sensor (VTEMP), and Battery power (VBAT)

- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for each EADC
- Maximum EADC clock frequency is 72 MHz for each EADC
- Up to 5.14 MSPS conversion rate for each EADC at the same time
- Configurable EADC internal sampling time for each EADC
- 12-bit, 10-bit, 8-bit, 6-bit configurable resolution for each EADC
- Supports calibration and load calibration words capability for each EADC
- Supports internal reference voltage VREF: 1.6V, 2.0V, 2.5V, and 3.0V.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
  - Up to 19 sample modules
  - Each of sample modules which is configurable for EADC converter channel (EADC0/1_CH0~15) and trigger source for each EADC
  - Sample module 16~18 is fixed for EADC0channel 16, 17, 18 input sources as band- gap voltage, temperature sensor, and battery power (VBAT)
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC0/1_SWTRG[n], n = 0~18)
  - External pin EADC0/1_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

4.29 Digital to Analog Converter (DAC)

4.29.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external

operational amplifier.

4.29.2 Features

- Analog output voltage range: 0~AVDD.
- Supports 12- or 8-bit output mode.
- Rail to rail settle time 6us.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), VREF pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

4.30 Analog Comparator Controller (ACMP)

4.30.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

4.30.2 Features

- Analog input voltage range: 0 ~ AVDD (voltage of AVDD pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
- Supports wake-up function
- Supports programmable propagation speed and low power consumption
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)

        - DAC0 output (DAC0_OUT)
        - ACMP1 supports
    - 4 multiplexed I/O pins at positive sources:
        - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
    - 4 negative sources:
        - ACMP1_N
        - Comparator Reference Voltage (CRV)
        - Internal band-gap voltage (VBG)
        - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode

4.31 Amplifier (OPA)

4.31.1 Overview

This device is equipped with three operational amplifiers. Users can enable each of them individually, by their application purpose. One of these OP amplifier outputs is connected to ADC channel for measurement requirement. The OP amplifier circuit also can be used in the application of Programmable Gain Amplifier (PGA).

4.31.2 Features

- Analog input voltage range: 0~VDD.
- Supports up to 3 operator amplifiers.
- Supports to use Schmitt trigger buffer output for simple comparator function.
- Supports to Schmitt trigger buffer output interrupts.

4.32 Peripherals Interconnection

4.32.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

4.32.2 Peripherals Interconnect Matrix Table

Source	Destination									
	BPWM	DAC	EADC	ECAP	EPWM	HIRC	IRCTRIM	HIRC48M	TIMERPWM	QEI
ACMP	-	-	-	-	3	-	-	-	3,6	
BOD	-	-	-	-	3	-	-	-	3	
BPWM	4	-	1	-	4	-	-	-	-	
Clock Fail	-	-	-	-	3	-	-	-	3	
CPU Lockup	-	-	-	-	3	-	-	-	3	
EADC	-	-	-	-	3	-	-	-	-	
EPWM	4	1	1	-	4	-	-	-	-	
IRCTRIM	-	-	-	-	-	2	-	2	-	
LIRC	-	-	-	-	-	-	-	-	6	
LXT	-	-	-	-	-	-	2	-	-	
QEI	-	-	-	8	-	-	-	-	-	
SRAM	-	-	-	-	3	-	-	-	3	
TIMERPWM	5	1	1	-	5	-	-	-	7	9
USB11Device	-	-	-	-	-	-	2	-	-	

Table 4.44-1 Peripherals Interconnect Matrix table

4.32.3 Functional Description

4.32.3.1 From EPWM, TIMER to EADC/DAC

EPWM Trigger EADC Conversion

EPWM can be one of the EADC conversion trigger source.

Setting the EADC external hardware trigger input source from EPWM trigger is described in TRM section 4.40.5.8.

EPWM Trigger DAC Conversion

EPWM can also be used to trigger DAC conversion.

Setting the DAC hardware trigger input source from EPWM trigger is described in TRM section 4.41.5.6.

The detailed EPWM trigger conditions are described in TRM section 4.12.5.27.

BPWM Trigger EADC Conversion

BPWM can be one of the EADC conversion trigger source.

Setting the EADC external hardware trigger input source from BPWM trigger is described in TRM section 4.40.5.8.
The detailed BPWM trigger conditions are described in TRM section 4.13.5.16.

Timer Trigger EADC Conversion

Timer0 ~ Timer3 can be one of the EADC conversion trigger source. When timer counter value matches the timer compared value or when the TMx_EXT pin edge transition meets setting, timer will trigger the ADC to start the conversion.
Setting the EADC external hardware trigger input source from timer trigger is described in TRM section 4.40.5.9.

Timer Trigger DAC Conversion

Setting the DAC hardware trigger input source from TIMER trigger is described in TRM section 4.41.5.6.
The detailed Timer trigger conditions are described in TRM section 4.8.5.10.

4.32.3.2 From LXT and USB 1.1 Device to HIRC TRIM & RC 48 MHz

Use LXT or USB Synchronous Mode to System Auto-trim HIRC Circuit

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator) and RC 48 MHz oscillator, according to the accurate external 32.768 kHz crystal oscillator or internal USB synchronous mode, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.
The detail of HIRC trim setting is described in section 4.2.9

4.1.1.1 From ACMP, BOD, Clock Fail, SRAM Parity Error and CPU Lockup to EPWM/ TIMERPWM

EPWM Brake Source

EPWM brake source can be ACMP0/1_O output signal or EADC result monitor or several different system fail conditions include clock fail, Brown-out detect, and Core lockup and SRAM Parity Error. When system fault, EPWM brake signal generated, EPWM output will be set to protect the power switch controlled by EPWM.
The detailed setting of EPWM brake function is described in TRM section 4.12.5.23.

TIMERPWM Brake Source

TIMERPWM brake source can be ACMP0/1_O output signal or several different system fail conditions include clock fail, Brown-out detect, and Core lockup and SRAM Parity Error. When system fault, EPWM brake signal generated, EPWM output will be set to protect the power switch controlled by EPWM.

The detailed setting of TIMERPWM brake function is described in TRM section 4.8.6.17.

4.32.3.3 From EPWM/ BPWM to EPWM/ BPWM

EPWM Synchronous Start Function

Select synchronous source from EPWM0 or EPWM1 or BPWM0 or BPWM1, and select EPWM channels. The chosen EPWM channels will start counting at the same time once the synchronous start function is enabled and CNTSEN(EPWM_SSTRG[0]) is set.

The detailed setting of EPWM synchronous start function is described in TRM section 4.12.5.19.

BPWM Synchronous Start Function

Select synchronous source from EPWM0 or EPWM1 or BPWM0 or BPWM1, and select BPWM channels. The chosen BPWM channels will start counting at the same time once the synchronous start function is enabled and CNTSEN(BPWM_SSTRG[0]) is set.

The detailed setting of BPWM synchronous start function is described in TRM section 4.13.5.11.

4.32.3.4 From TIMER to EPWM/BPWM

Timer Generates Trigger Pulses as EPWM External Clock Source

Timer0 ~ Timer3 can generates trigger pules as EPWM/BPWM external clock source.

When timer counter value matches the timer compared value or when the TMx_EXT pin edge transition meets setting, timer can generate a trigger pulse by setting described in TRM section 6.8.5.10.

The setting of EPWM/BPWM clock source is described in TRM section 4.13.3 / 4.12.3.

4.32.3.5 From ACMP and LIRC to Timer Capture Function

Measure the Time Interval of ACMP0/1 Output Signal or LIRC Clock Speed

Sets the timer capture source from ACMP0/1 output signal or LIRC clock and measures the time interval of the signal by using timer capture function. Users can

use the results of time interval to trim LIRC through software or to get the ACMP0/1 output pulse width.
The detail of time capture function setting is described in TRM section 4.8.5.8 and 4.8.5.9.

4.32.3.6 From Timer0/2 to Timer1/3

Inter-Timer Trigger Capture Mode

Timer0/2 will be forced in event counting mode, counting with external event, and will generate an internal signal (INTR_TMR_TRG) to trigger Timer1/3 start or stop counting. The Timer1/3 will be forced in capture mode and start/stop trigger-counting by Timer0/2 counter status.
The detail of inter-timer trigger capture mode is described in TRM section 4.8.5.11.

4.32.3.7 From QEI to ECAP

ECAP Input Noise Filter

The architecture of ECAP input noise filter is similar to that one used for QEI. With 6 sampling-rate options, it supports a wide range of filtering noise, the duration of filtered noise and the duration of the signal that is guaranteed to be sampled.
The detailed setting of modulation is described in TRM section 4.14.5.1.

4.32.3.8 From TIMER to QEI

TIMER TIF Event to QEI

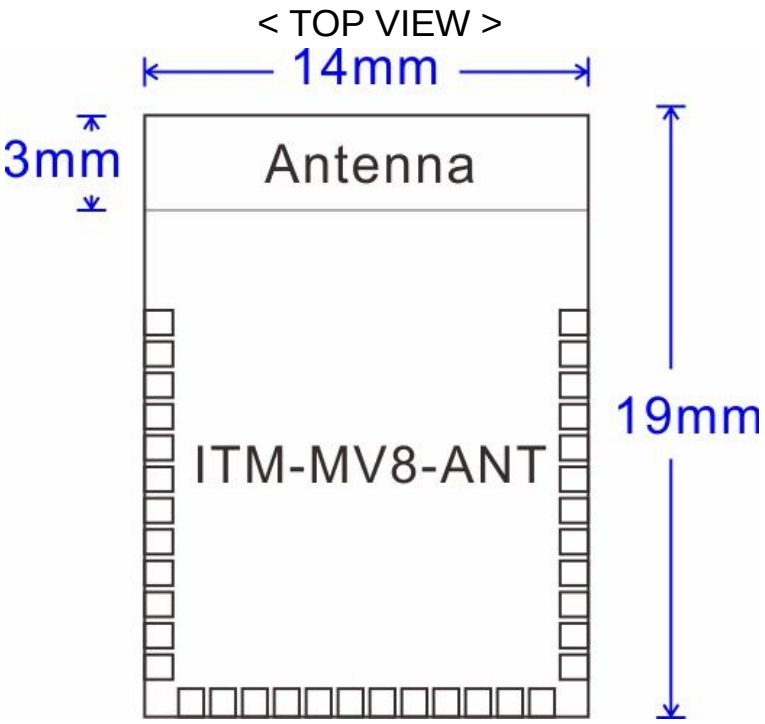
When QEI bit HOLDCNT(QEI_CTL[24]) set, the CNT(QEI_CNT[31:0]) content will be captured into QEI Counter Hold Register CNTHOLD(QEI_CNTHOLD[31:0]), the data will be held until the next

HOLDCNT (QEI_CTL[24]) trigger comes. The bit HOLDCNT can be set by writing 1 to it or the rising edge of timers interrupt flags TIF (TIMERx_INTSTS[0])The detailed setting of modulation is described in TRM section 4.14.5.11.
The detailed setting of modulation is described in TRM section 4.8.5.1.

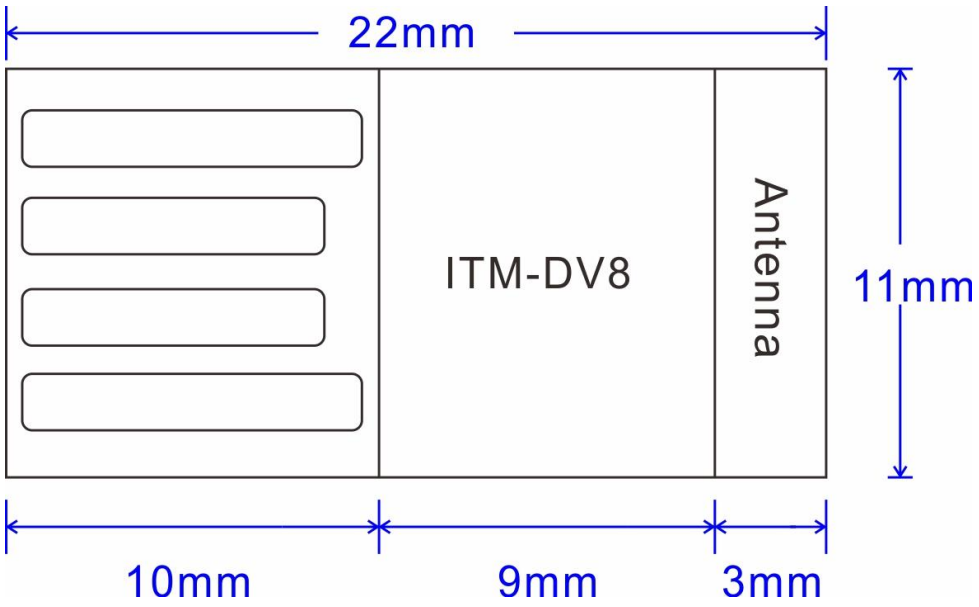
5. Pin Assignments

5.1 PCB Pin Outline

ITM-MV8-ANT (14mm x 19mm x 2.2mm)



ITM-DV8 (22mm x 11mm x 2.0mm)



5.2 Pin Definition

ITM-MV8-ANT

Pin No.	Pin-Define	Type	Description
1	RFIO	AIO	RF pin
2	GND	G	Ground
3	PA.9	DIO	Multi-functional I/O pin.
4	PA.8	DIO	Multi-functional I/O pin
5	PA.7	DIO	Multi-functional I/O pin
6	PA.6	DIO	Multi-functional I/O pin
7	PA.5	DIO	Multi-functional I/O pin
8	PA.4	DIO	Multi-functional I/O pin
9	PA.3	DIO	Multi-functional I/O pin;(ROLLER_B)
10	PA.2	DIO	Multi-functional I/O pin;(ROLLER_A)
11	PA.1	DIO	Multi-functional I/O pin;(BNT_R)
12	PA.0	DIO	Multi-functional I/O pin;(BNT_L)
13	PF.0/ICE_DAT	DIO	Multi-functional I/O pin;(MCU_ICE_DAT)
14	PF.1/ICE_CLK	DIO	Multi-functional I/O pin;(MCU_ICE_CLK)
15	PC.5	DIO	Multi-functional I/O pin
16	PC.4	DIO	Multi-functional I/O pin
17	PC.3	DIO	Multi-functional I/O pin
18	PC.2	DIO	Multi-functional I/O pin;(RT_SHOUTDOWN)
19	PC.1	DIO	Multi-functional I/O pin;(BNT_ROLLER)
20	PC.0	DIO	Multi-functional I/O pin;(WAKEUP)
21	PA.12/SPI2_CS	DIO	Multi-functional I/O pin;(SPI2_CS)
22	PA.13/SPI2_CLK	DIO	Multi-functional I/O pin;(SPI2_CLK)
23	PA.14/SPI2_MISO	DIO	Multi-functional I/O pin;(SPI2_MISO)
24	PA.15/ SPI2_MOSI	DIO	Multi-functional I/O pin;(SPI2_MOSI)
25	nRESET	DI	Module reset pin (Low to reset module)
26	VDD	P	3.3V Power supply
27	PC.14	DIO	Multi-functional I/O pin
28	PB.15	DIO	Multi-functional I/O pin
29	PB.14	DIO	Multi-functional I/O pin
30	PB.13/UART0_TX	DIO	Multi-functional I/O pin;(UART0_TX)
31	PB.12/UART0_RX	DIO	Multi-functional I/O pin;(UART0_RX)
32	PB.7	DIO	Multi-functional I/O pin
33	PB.6	DIO	Multi-functional I/O pin
34	PA.11	DIO	Multi-functional I/O pin

35	PA.10	DIO	Multi-functional I/O pin
36	GND	G	Ground pin.

ITM-DV8

Pin No.	Pin-Define	Type	Description
1	VDD	P	USB 5V Power Supply
2	USB_DN	AIO	USB Negative Differential Signal Pin
3	USB_DP	AIO	USB Positive Differential Signal Pin.
4	GND	G	Ground

5.3 Pin Configuration (ITM-MV8-ANT)

Users can configure the multiple-functional I/O pin of ITM-MV8-ANT to fit their application. The I/O configuration table is shown as below.

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)
PA.0 / MFP0 means SYS_GPA_MFPL[3:0] = 0x0.
PA.9 / MFP5 means SYS_GPA_MFPH[7:4] = 0x5.

Pin No.	Pin-Define	Type	MFP	Description
3	PA.9	I/O	MFP0	General purpose digital I/O pin.
	OPA1_N	A	MFP1	Operational amplifier 1 negative input pin.
	EBI_MCLK	O	MFP2	EBI external clock output pin.
	SPI2_MISO	I/O	MFP4	SPI2 MISO (Master In, Slave Out) pin.
	SD1_DAT1	I/O	MFP5	SD/SDIO1 data line bit 1.
	USCI0_DAT1	I/O	MFP6	USCI0 data 1 pin.
	UART1_TXD	O	MFP7	UART1 data transmitter output pin.
	BPWM0_CH2	I/O	MFP9	BPWM0 channel 2 output/capture input.
	QEI1_A	I	MFP10	Quadrature encoder 1 phase A input
	ECAP0_IC1	I	MFP11	Enhanced capture unit 0 input 1 pin.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
4	PA.8	I/O	MFP0	General purpose digital I/O pin.
	OPA1_P	A	MFP1	Operational amplifier 1 positive input pin.
	EBI_ALE	O	MFP2	EBI address latch enable output pin.
	SPI2_MOSI	I/O	MFP4	SPI2 MOSI (Master Out, Slave In) pin.
	SD1_DAT0	I/O	MFP5	SD/SDIO1 data line bit 0.
	USCI0_CTL1	I/O	MFP6	USCI0 control 1 pin.

	UART1_RXD	I	MFP7	UART1 data receiver input pin.
	BPWM0_CH3	I/O	MFP9	BPWM0 channel 3 output/capture input.
	QEI1_B	I	MFP10	Quadrature encoder 1 phase B input
	ECAP0_IC2	I	MFP11	Enhanced capture unit 0 input 2 pin.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
	INT4	I	MFP15	External interrupt 4 input pin.
5	PA.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD7	I/O	MFP2	EBI address/data bus bit 7.
	SPI1_CLK	I/O	MFP4	SPI1 serial clock pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I2C1 clock pin.
	EPWM1_CH4	I/O	MFP11	EPWM1 channel 4 output/capture input.
	BPWM1_CH2	I/O	MFP12	BPWM1 channel 2 output/capture input.
	ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
6	PA.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD6	I/O	MFP2	EBI address/data bus bit 6.
	SPI1_SS	I/O	MFP4	SPI1 slave select pin.
	SD1_nCD	I	MFP5	SD/SDIO1 card detect input pin
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
	EPWM1_CH5	I/O	MFP11	EPWM1 channel 5 output/capture input.
	BPWM1_CH3	I/O	MFP12	BPWM1 channel 3 output/capture input.
	ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
7	PA.5	I/O	MFP0	General purpose digital I/O pin.
	SPIM_D2	I/O	MFP2	SPIM data 2 pin for Quad Mode I/O.
	QSPI0_MISO1	I/O	MFP3	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	SD1_CMD	I/O	MFP5	SD/SDIO1 command/response pin
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	UART5_TXD	O	MFP8	UART5 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
	EPWM0_CH0	I/O	MFP13	EPWM0 channel 0 output/capture input.
	QEI0_INDEX	I	MFP14	Quadrature encoder 0 index input

8	PA.4	I/O	MFP0	General purpose digital I/O pin.
	SPIM_D3	I/O	MFP2	SPIM data 3 pin for Quad Mode I/O.
	QSPI0_MOSI1	I/O	MFP3	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	SD1_CLK	O	MFP5	SD/SDIO1 clock output pin
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	UART5_RXD	I	MFP8	UART5 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
	EPWM0_CH1	I/O	MFP13	EPWM0 channel 1 output/capture input.
	QEI0_A	I	MFP14	Quadrature encoder 0 phase A input
9	PA.3	I/O	MFP0	General purpose digital I/O pin.
	SPIM_SS	I/O	MFP2	SPIM slave select pin.
	QSPI0_SS	I/O	MFP3	Quad SPI0 slave select pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	SD1_DAT3	I/O	MFP5	SD/SDIO1 data line bit 3.
	UART4_TXD	O	MFP7	UART4 data transmitter output pin.
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
	EPWM0_CH2	I/O	MFP13	EPWM0 channel 2 output/capture input.
	QEI0_B	I	MFP14	Quadrature encoder 0 phase B input
10	PA.2	I/O	MFP0	General purpose digital I/O pin.
	SPIM_CLK	I/O	MFP2	SPIM serial clock pin.
	QSPI0_CLK	I/O	MFP3	Quad SPI0 serial clock pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	SD1_DAT2	I/O	MFP5	SD/SDIO1 data line bit 2.
	UART4_RXD	I	MFP7	UART4 data receiver input pin.
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	MFP13	EPWM0 channel 3 output/capture input.
11	PA.1	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP2	SPIM MISO (Master In, Slave Out) pin.
	QSPI0_MISO0	I/O	MFP3	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	SD1_DAT1	I/O	MFP5	SD/SDIO1 data line bit 1.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.

	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	I2C2_SCL	I/O	MFP9	I2C2 clock pin.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
	EPWM0_CH4	I/O	MFP13	EPWM0 channel 4 output/capture input.
	DAC1_ST	I	MFP15	DAC1 external trigger input.
12	PA.0	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP2	SPIM MOSI (Master Out, Slave In) pin.
	QSPI0_MOSI0	I/O	MFP3	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	SD1_DAT0	I/O	MFP5	SD/SDIO1 data line bit 0.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	I2C2_SDA	I/O	MFP9	I2C2 data input/output pin.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
	EPWM0_CH5	I/O	MFP13	EPWM0 channel 5 output/capture input.
	DAC0_ST	I	MFP15	DAC0 external trigger input.
13	PF.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP3	I2C1 clock pin.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	ICE_DAT	O	MFP14	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
14	PF.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	ICE_CLK	I	MFP14	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
15	PC.5	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD5	I/O	MFP2	EBI address/data bus bit 5.
	SPIM_D2	I/O	MFP3	SPIM data 2 pin for Quad Mode I/O.
	QSPI0_MISO1	I/O	MFP4	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	UART4_TXD	O	MFP11	UART4 data transmitter output pin.
	EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
16	PC.4	I/O	MFP0	General purpose digital I/O pin.

	EBI_AD4	I/O	MFP2	EBI address/data bus bit 4.
	SPIM_D3	I/O	MFP3	SPIM data 3 pin for Quad Mode I/O.
	QSPI0_MOSI1	I/O	MFP4	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	UART4_RXD	I	MFP11	UART4 data receiver input pin.
	EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
17	PC.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD3	I/O	MFP2	EBI address/data bus bit 3.
	SPIM_SS	I/O	MFP3	SPIM slave select pin.
	QSPI0_SS	I/O	MFP4	Quad SPI0 slave select pin.
	SPI1_MISO	I/O	MFP7	SPI1 MISO (Master In, Slave Out) pin.
	UART2_nRTS	O	MFP8	UART2 request to Send output pin.
	I2C0_SMBAL	O	MFP9	I2C0 SMBus SMBALTER pin
	UART3_TXD	O	MFP11	UART3 data transmitter output pin.
	EPWM1_CH2	I/O	MFP12	EPWM1 channel 2 output/capture input.
18	PC.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD2	I/O	MFP2	EBI address/data bus bit 2.
	SPIM_CLK	I/O	MFP3	SPIM serial clock pin.
	QSPI0_CLK	I/O	MFP4	Quad SPI0 serial clock pin.
	SPI1_MOSI	I/O	MFP7	SPI1 MOSI (Master Out, Slave In) pin.
	UART2_nCTS	I	MFP8	UART2 clear to Send input pin.
	I2C0_SMBSUS	O	MFP9	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	UART3_RXD	I	MFP11	UART3 data receiver input pin.
	EPWM1_CH3	I/O	MFP12	EPWM1 channel 3 output/capture input.
19	PC.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD1	I/O	MFP2	EBI address/data bus bit 1.
	SPIM_MISO	I/O	MFP3	SPIM MISO (Master In, Slave Out) pin.
	QSPI0_MISO0	I/O	MFP4	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	SPI1_CLK	I/O	MFP7	SPI1 serial clock pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.
20	PC.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD0	I/O	MFP2	EBI address/data bus bit 0.

	SPIM_MOSI	I/O	MFP3	SPIM MOSI (Master Out, Slave In) pin.
	QSPI0_MOSI0	I/O	MFP4	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	SPI1_SS	I/O	MFP7	SPI1 slave select pin.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
21	PA.12	I/O	MFP0	General purpose digital I/O pin.
	UART4_TXD	O	MFP3	UART4 data transmitter output pin.
	I2C1_SCL	I/O	MFP4	I2C1 clock pin.
	SPI2_SS	I/O	MFP5	SPI2 slave select pin.
	BPWM1_CH2	I/O	MFP11	BPWM1 channel 2 output/capture input.
	QEI1_INDEX	I	MFP12	Quadrature encoder 1 index input
	USB_VBUS	P	MFP14	Power supply from USB host or HUB.
22	PA.13	I/O	MFP0	General purpose digital I/O pin.
	UART4_RXD	I	MFP3	UART4 data receiver input pin.
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
	SPI2_CLK	I/O	MFP5	SPI2 serial clock pin.
	BPWM1_CH3	I/O	MFP11	BPWM1 channel 3 output/capture input.
	QEI1_A	I	MFP12	Quadrature encoder 1 phase A input
23	PA.14	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	SPI2_MISO	I/O	MFP5	SPI2 MISO (Master In, Slave Out) pin.
	I2C2_SCL	I/O	MFP6	I2C2 clock pin.
	BPWM1_CH4	I/O	MFP11	BPWM1 channel 4 output/capture input.
	QEI1_B	I	MFP12	Quadrature encoder 1 phase B input
24	PA.15	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	SPI2_MOSI	I/O	MFP5	SPI2 MOSI (Master Out, Slave In) pin.
	I2C2_SDA	I/O	MFP6	I2C2 data input/output pin.
	BPWM1_CH5	I/O	MFP11	BPWM1 channel 5 output/capture input.
	EPWM0_SYNC_IN	I	MFP12	EPWM0 counter synchronous trigger input pin.
27	PC.14	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
	USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
	QSPI0_CLK	I/O	MFP6	Quad SPI0 serial clock pin.

	EPWM0_SYNC_IN	I	MFP11	EPWM0 counter synchronous trigger input pin.
	TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
28	PB.15	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH15	A	MFP1	EADC0 channel 15 analog input.
	EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	USCI0_CTL1	I/O	MFP5	USCI0 control 1 pin.
	UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	I2C2_SMBAL	O	MFP8	I2C2 SMBus SMBALTER pin
	EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
29	PB.14	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH14	A	MFP1	EADC0 channel 14 analog input.
	EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	USCI0_DAT1	I/O	MFP5	USCI0 data 1 pin.
	UART0_nRTS	O	MFP6	UART0 request to Send output pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	I2C2_SMBSUS	O	MFP8	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
	EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	CLKO	O	MFP14	Clock Out
30	PB.13	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH13	A	MFP1	EADC0 channel 13 analog input.
	DAC1_OUT	A	MFP1	DAC1 channel analog output.
	ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.
	ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
	EBI_AD14	I/O	MFP2	EBI address/data bus bit 14.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	USCI0_DAT0	I/O	MFP5	USCI0 data 0 pin.
	UART0_TXD	O	MFP6	UART0 data transmitter output pin.
	UART3_nRTS	O	MFP7	UART3 request to Send output pin.
	I2C2_SCL	I/O	MFP8	I2C2 clock pin.
	EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
31	PB.12	I/O	MFP0	General purpose digital I/O pin.

	EADC0_CH12	A	MFP1	EADC0 channel 12 analog input.
	DAC0_OUT	A	MFP1	DAC0 channel analog output.
	ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
	ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.
	EBI_AD15	I/O	MFP2	EBI address/data bus bit 15.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	USCI0_CLK	I/O	MFP5	USCI0 clock pin.
	UART0_RXD	I	MFP6	UART0 data receiver input pin.
	UART3_nCTS	I	MFP7	UART3 clear to Send input pin.
	I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
	SD0_nCD	I	MFP9	SD/SDIO0 card detect input pin
	EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
32	PB.7	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH7	A	MFP1	EADC0 channel 7 analog input.
	EBI_nWRL	O	MFP2	EBI low byte write enable output pin.
	USCI1_DAT0	I/O	MFP4	USCI1 data 0 pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	SD1_CMD	I/O	MFP7	SD/SDIO1 command/response pin
	EBI_nCS0	O	MFP8	EBI chip select 0 output pin.
	BPWM1_CH4	I/O	MFP10	BPWM1 channel 4 output/capture input.
	EPWM1_BRAKE0	I	MFP11	EPWM1 Brake 0 input pin.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	INT5	I	MFP13	External interrupt 5 input pin.
	ACMP0_O	O	MFP15	Analog comparator 0 output pin.
33	PB.6	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH6	A	MFP1	EADC0 channel 6 analog input.
	EBI_nWRH	O	MFP2	EBI high byte write enable output pin
	USCI1_DAT1	I/O	MFP4	USCI1 data 1 pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	SD1_CLK	O	MFP7	SD/SDIO1 clock output pin
	EBI_nCS1	O	MFP8	EBI chip select 1 output pin.
	BPWM1_CH5	I/O	MFP10	BPWM1 channel 5 output/capture input.
	EPWM1_BRAKE1	I	MFP11	EPWM1 Brake 1 input pin.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	INT4	I	MFP13	External interrupt 4 input pin.
	ACMP1_O	O	MFP15	Analog comparator 1 output pin.

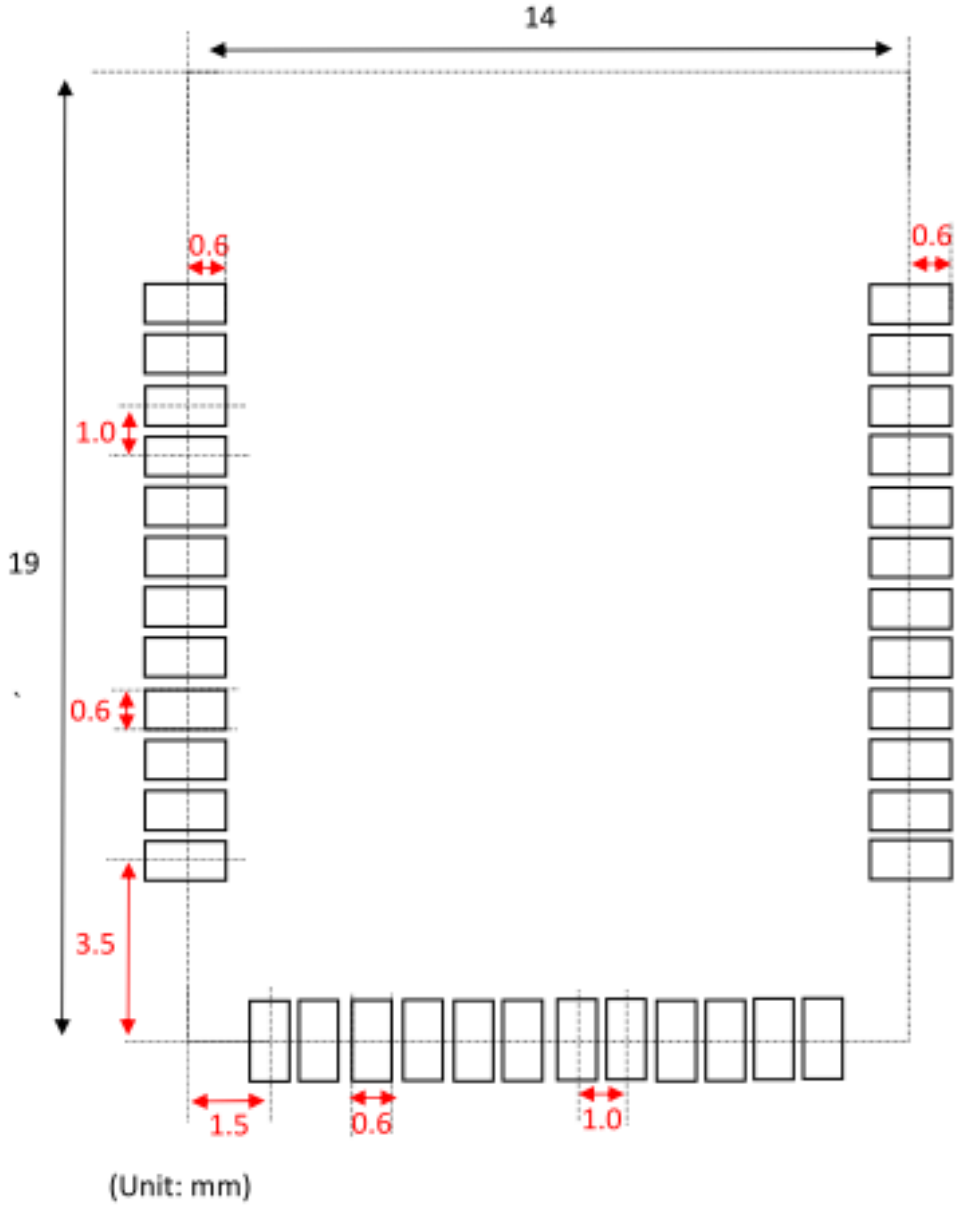
34	PA.11	I/O	MFP0	General purpose digital I/O pin.
	ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
	EBI_nRD	O	MFP2	EBI read enable output pin.
	SPI2_SS	I/O	MFP4	SPI2 slave select pin.
	SD1_DAT3	I/O	MFP5	SD/SDIO1 data line bit 3.
	USCI0_CLK	I/O	MFP6	USCI0 clock pin.
	I2C2_SCL	I/O	MFP7	I2C2 clock pin.
	BPWM0_CH0	I/O	MFP9	BPWM0 channel 0 output/capture input.
	EPWM0_SYNC_OUT	O	MFP10	EPWM0 counter synchronous trigger output pin.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
	DAC1_ST	I	MFP14	DAC1 external trigger input.
35	PA.10	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
	OPA1_O	A	MFP1	Operational amplifier 1 output pin.
	EBI_nWR	O	MFP2	EBI write enable output pin.
	SPI2_CLK	I/O	MFP4	SPI2 serial clock pin.
	SD1_DAT2	I/O	MFP5	SD/SDIO1 data line bit 2.
	USCI0_DAT0	I/O	MFP6	USCI0 data 0 pin.
	I2C2_SDA	I/O	MFP7	I2C2 data input/output pin.
	BPWM0_CH1	I/O	MFP9	BPWM0 channel 1 output/capture input.
	QEI1_INDEX	I	MFP10	Quadrature encoder 1 index input
	ECAP0_IC0	I	MFP11	Enhanced capture unit 0 input 0 pin.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	DAC0_ST	I	MFP14	DAC0 external trigger input.

6. Dimensions

6.1 Layout Recommendation

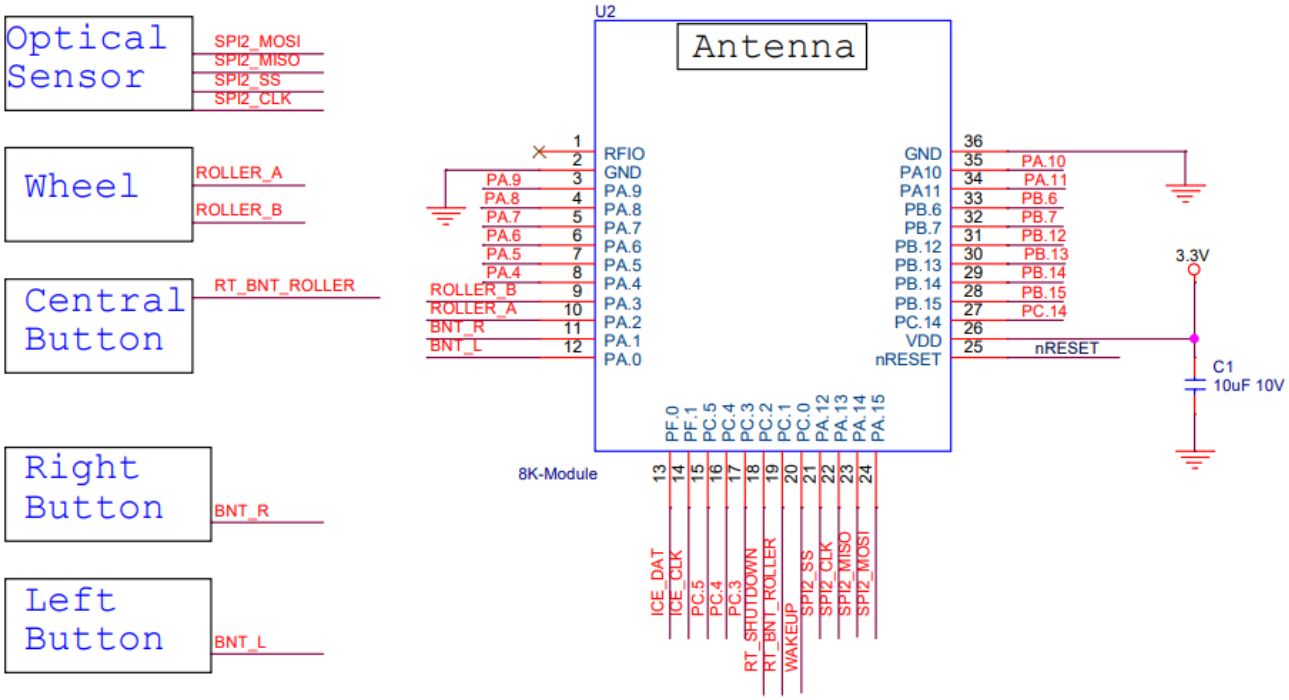
ITM-MV8-ANT

< TOP VIEW >



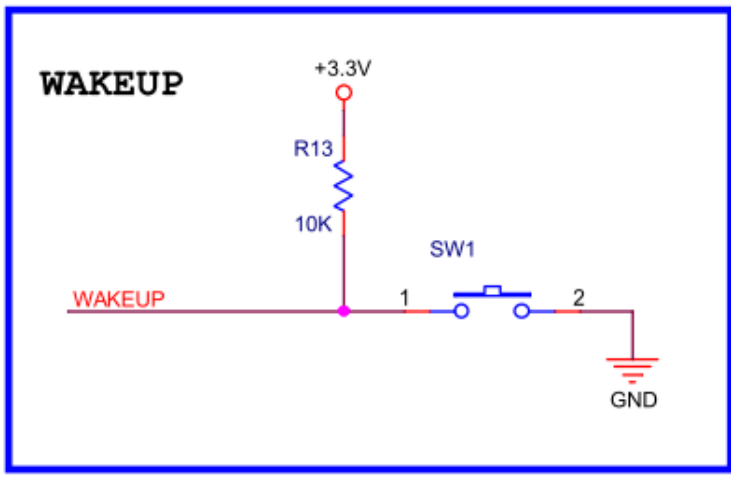
7. Reference Design

7.1 ITM-MV8-ANT



7.2 ITM-MV8 series module External Wake Up from Deep Sleep

This chart shows how to wake it with an external wake up, like a button press.



To test this example, wire a pushbutton to your ITM-MV8 series module by following the schematic diagram. The button is connected to PC.0（Wakeup pin） using a pull high 10k Ohm resistor.

8. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times